



MOTOROLA



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FACT DATA



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FACT DATA


Prepared by
Technical Information Center

This data book presents advanced information on Motorola's very high-speed, low-power advanced CMOS logic family.

FACT utilizes a sub 2 micron silicon gate CMOS process to attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic, namely, ultra low power and high noise immunity. As an added benefit, FACT offers the system designer superior line driving characteristics and excellent ESD and latchup immunity.

The FACT family consists of devices in two categories:

1. **AC**, standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
2. **ACT**, standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

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Alphanumeric Index of Devices

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Functional Selection

Abbreviations

S = Synchronous
A = Asynchronous
B = Both Synchronous and Asynchronous

2S = 2-State Output
3S = 3-State Output

N = Available Now
P = Planned (See FACT Selector Guide, SG-122 for latest availability status)

Inverters

Description	Type of Output	No.	AC	ACT
Hex	2S	04	N	N

AND Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	08	N	N
Triple 3-Input	2S	11	N	N

NAND Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	00	N	N
Triple 3-Input	2S	10	N	N

OR Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	32	N	N

NOR Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	02	N	N

Exclusive OR/NOR Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input XOR	2S	86	N	N
Quad 2-Input XNOR	2S	810	N	N

Schmitt Triggers

Description	Type of Output	No.	AC	ACT
Hex, Inverting	2S	14	N	N
NAND Gate, Quad 2-Input	2S	132	N	N

Flip-Flops

Description	Clock Edge	No.	AC	ACT
Dual D w/Set & Clear	Pos	74	N	N
Dual JK w/Set & Clear	Pos	109	N	N
8-Bit D, Non-Inverting	Pos	825	P	P

Multiplexers

Description	Type of Output	No.	AC	ACT
Quad 2-to-1, Non-Inverting	2S	157	N	N
	3S	257	P	P
Quad 2-to-1, Inverting	2S	158	P	P
	3S	258	N	N
Dual 4-to-1, Non-Inverting	2S	153	N	N
	3S	253	N	N
Dual 4-to-1, Inverting	2S	352	P	N
	3S	353	N	N
8-to-1	2S	151	P	N
	3S	251	P	N

Decoders/Demultiplexers

Description	Type of Output	No.	AC	ACT
Dual 1-of-4	2S	139	N	N
1-of-8	2S	138	N	N

Latches

Description	No. of Bits	Type of Output	No.	AC	ACT
Transparent, Non-Inverting	8	3S	373	N	N
	9	3S	843	P	P
	9	3S	845	P	P
Octal, Non-Inverting	8	3S	573	P	P
Transparent, Inverting	8	3S	533	P	P
	8	3S	563	P	P
Dual 4-Bit Addressable	8	2S	256	P	P
Addressable	8	2S	259	N	P

Shift Registers

Description	No. of Bits	Type of Output	Mode*				No.	AC	ACT
			SR	SL	Hold	Reset			
Parallel In-Parallel Out, Bidirectional	4	2S	X	X	X	A	194	P	P
	8	3S	X	X	X	S	323	P	P

* SR = Shift Right
SL = Shift Left

**Asynchronous Counters —
Negative Edge-Triggered**

Description	Load	Set	Reset	No.	AC	ACT
14-Stage Binary			X	4020	N	
12-Stage Binary			X	4040	N	

Buffers/Line Drivers

Description	Type of Output	No.	AC	ACT
Octal, Non-Inverting	3S	241	P	N
	3S	244	N	N
Bus Pinout	3S	541	N	N
Octal, Inverting	3S	240	N	N
Bus Pinout	3S	540	N	N

Transceivers

Description	Type of Output	No.	AC	ACT
Octal, Non-Inverting	3S	245	N	N
	3S	623	P	P
	3S	640	N	N
Octal, Inverting	3S	620	P	P
	3S	643	P	P
Octal, Non-Inverting with Register Mux Latch	3S	646	N	P
Octal, Inverting with Register Mux Latch	3S	648	P	P

MSI Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	Clock Enable	No.	AC	ACT
D-Type, Non-Inverting	4	2S		X	377	N	N
	6	2S	A		174	N	P
	6	2S		X	378	N	N
	8	2S	A		273	N	N
	8	3S			574	P	P
	8	3S			564	P	P
D-Type, Inverting							

**Cascadable Synchronous Counters —
Positive Edge-Triggered**

Description	Type of Output	Load	Reset	No.	AC	ACT
Decade	2S	S	A	160	P	N
	2S	S	S	162	P	N
Decade, Up/Down	2S	A		190	N	P
	3S	S	B	568	P	P
4-Bit Binary	2S	S	A	161	P	P
	2S	S	S	163	N	P
4-Bit Binary, Up/Down	3S	S	B	569	P	P

Comparators

Description	Type of Output	P=Q	P>Q	P<Q	No.	AC	ACT
4-Bit Identity	2S	X			521	P	P

Arithmetic Operators

Description	Type of Output	No.	AC	ACT
4-Bit Barrel Shifter	3S	350	P	P

Description	Type of Output	No. of Bits	Mode				No. of Bits	AC	ACT
			SR	SR	SR	SR			
Transfer to Parallel Out Registers	1	32	X	X	X	X	192	P	P
			X	X	X	X	192	P	P

SR = Shift Register
SR = Shift Register

Asynchronous Counters --									
Negative Edge-Triggered									
Description									
12 Stage Binary			X				4096	N	
12 Stage Binary			X				4096	N	

Synchronous Drivers									
Description									
Output Non-Inverting			32				256	P	N
Output Inverting			32				256	P	N
Bus Present			32				256	N	N
Output Inverting			32				256	N	N
Bus Present			32				256	N	N

Transceivers									
Description									
Output Non-Inverting			32				256	N	N
Output Inverting			32				256	N	N
Output Non-Inverting with Register Mask Enable			32				256	N	N
Output Inverting with Register Mask Enable			32				256	N	N

Arithmetic Operators									
Description									
4 Bit Binary			32				256	P	P

Combinational									
Description									
4 Bit Binary			32				256	P	P

Asynchronous Counters --									
Positive Edge-Triggered									
Description									
12 Stage Binary			32				4096	N	
12 Stage Binary			32				4096	N	

MSI Flip-Flop Registers									
Description									
D-Type Non-Inverting			32				256	N	N
D-Type Inverting			32				256	N	N
J-K			32				256	N	N
S-R			32				256	N	N
T			32				256	N	N
D-Type Inverting			32				256	N	N

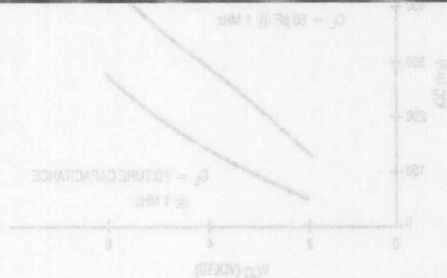
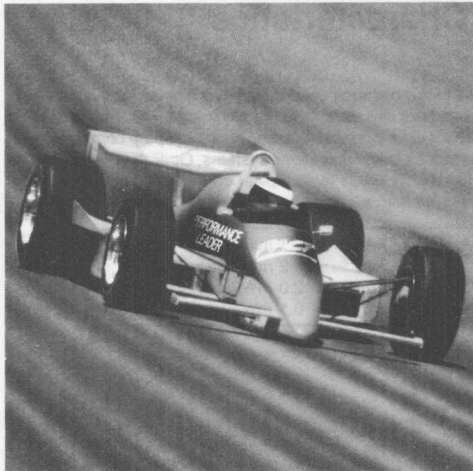


Figure 2-1. t_{PD} versus V_{CC}

Figure 2-1 illustrates the effects of V_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and 100 pF. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

FACT	= 8.0 ns @ $C_L = 50$ pF
ALS	= 12.0 ns @ $C_L = 50$ pF
LS	= 22.0 ns @ $C_L = 15$ pF
HC	= 17.5 ns @ $C_L = 50$ pF

AC performance specifications are guaranteed at 5 ± 0.5 V and 3.3 ± 0.3 V. For worst case design at 2.5 ± 0.3 V, the formula below can be used to determine AC performance.

AC performance at 2.5 ± 0.3 V: $t_{PD} = 1.9 \times AC$ specification at 3.3 V.

FACT DATA

2-5

FACT Descriptions and Family

FACT — Logic

Motrols FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fan-out capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies. The sub-micron silicon gate CMOS process utilized in this family has been proven in the field. It has been further enhanced to meet and exceed the JEDEC standards for MAXXX logic.

For direct replacement of LS, ALS and other TTL devices, the FACT family with TTL-type input thresholds are included in the FACT family. These include the most common bus and output drivers.

- Full Logic Product Line
- Industry Standard Functions and Pinouts for 801, MS1 and LS1
- Meets or Exceeds JEDEC Standards for MAXXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
- Common Output Structure for Standard and Buffer Drivers
- Output Sink/Source Current of 24 mA
- Transmission Line Driving 50 ohm (Commercial)
- Guaranteed
- Operation from -55 to $+125$ °C
- Temperature Range -40 °C to $+85$ °C (Commercial)
- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range ($V_{CC} = 2$ to 6 Vdc) and sufficient current drive to interface with most other logic families available today.

Device designers are as follows:

FACT — This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive 24 mA of I_{OH} and I_{OL} current. Industry standard AC noninverting and pinouts are used.

FACT — This is a high-speed CMOS device with a TTL-type CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a $V_{CC} = 5$ V ± 0.5 V with $V_{OH} = 2.4$ V and $V_{OL} = 0.4$ V. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. FACT devices have the same output structure as FACT devices.

Low Power CMOS Operation

There is one single characteristic that justifies the existence of CMOS: it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system

FACT Descriptions and Family Characteristics

FACT — Logic

Motorola FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fan-out capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The sub two-micron silicon gate CMOS process utilized in this family has been proven in the field. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 74ACTXXX devices.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
 - Common Output Structure for Standard and Buffer Drivers
 - Output Sink/Source Current of 24 mA
 - Transmission Line Driving 50 ohm (Commercial) Guaranteed
- Operation from 2–6 Volts Guaranteed
- Temperature Range -40°C to $+85^{\circ}\text{C}$ (Commercial)
- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range ($V_{CC} = 2$ to 6 Vdc) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC — This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ± 24 mA of I_{OH} and I_{OL} current. Industry standard 'AC nomenclature and pinouts are used.

'ACT — This is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ with $V_{OH} = 2.4\text{ V}$ and $V_{OL} = 0.4\text{ V}$. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as 'AC devices.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system

reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT	= 0.1 mW/Gate
ALS	= 1.2 mW/Gate
LS	= 2.0 mW/Gate
HC	= 0.1 mW/Gate

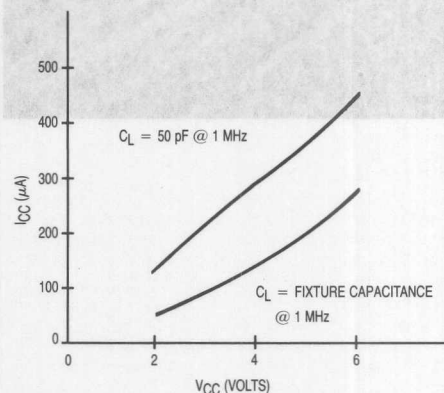


Figure 2-1. I_{CC} versus V_{CC}

Figure 2-1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

FACT	= 6.0 ns @ $C_L = 50\text{ pF}$
ALS	= 12.0 ns @ $C_L = 50\text{ pF}$
LS	= 22.0 ns @ $C_L = 15\text{ pF}$
HC	= 17.5 ns @ $C_L = 50\text{ pF}$

AC performance specifications are guaranteed at $5\text{ V} \pm 0.5\text{ V}$ and $3.3\text{ V} \pm 0.3\text{ V}$. For worst case design at 2 V V_{CC} on all device types, the formula below can be used to determine AC performance.

AC performance at 2 V $V_{CC} = 1.9 \times$ AC specification at 3.3 V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and $5\text{ V} \pm 10\% V_{CC}$.

Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|$ or $|V_{IH} - V_{OH}|$ at $4.5\text{ V } V_{CC}$.

FACT	= 1.25/1.25 V
ALS	= 0.4/0.7 V
LS	= 0.3/0.7 V @ $4.75\text{ V } V_{CC}$
HC	= 0.8/1.25 V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC' and 'ACT' device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All devices ('AC' or 'ACT') are guaranteed to source and sink 24 mA . Commercial devices, 74AC/ACTXXX, are capable of driving 50 ohm transmission lines.

I_{OL}/I_{OH} Characteristics

FACT	= 24/-24 mA
ALS	= 24/-15 mA
LS	= 8/-0.4 mA @ $4.75\text{ V } V_{CC}$
HC	= 4/-4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied 'typical' output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these 'typical' performance values across the operating voltage and temperature limits. Fortunately for the system designers, Motorola has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 ohms for the commercial temperature range.

Figure 2-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{out} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{out} < 0$), are the curves for V_{OL} and I_{IL} . Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

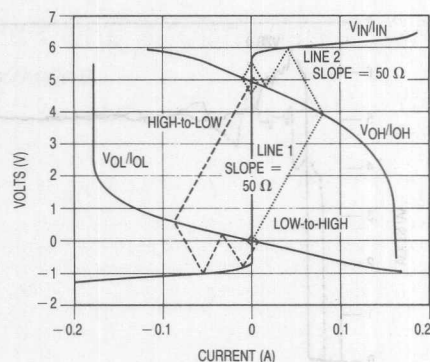


Figure 2-2. Gate Driving 50 Ohm Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV . Then draw a 50 ohm load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95 V . Then draw a line with a slope of -50 ohms from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figures 2-3a, 2-3b, 2-3c and 2-3d show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

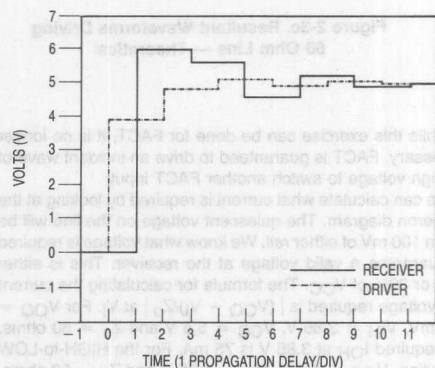


Figure 2-3a. Resultant Waveforms Driving 50 Ohm Line — Theoretical

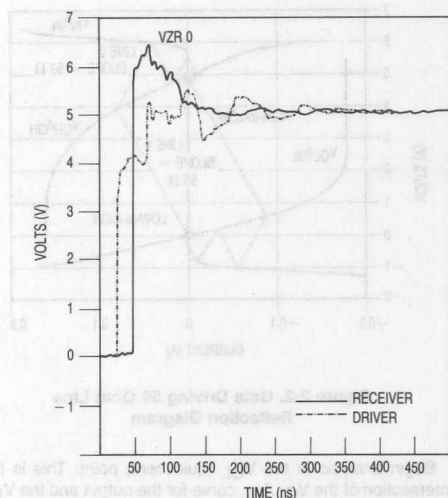


Figure 2-3b. Resultant Waveforms Driving 50 Ohm Line — Actual

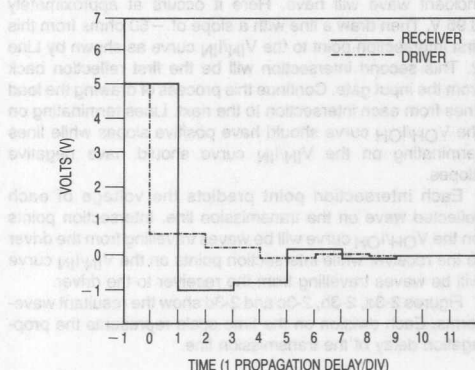


Figure 2-3c. Resultant Waveforms Driving 50 Ohm Line — Theoretical

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC} . The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_0|$ at V_I . For $V_{OQ} = 100$ mV, $V_{IH} = 3.85$ V, $V_{CC} = 5.5$ V and $Z_0 = 50$ ohms, the required I_{OH} at 3.85 V is 75 mA. For the HIGH-to-LOW transition, $V_{OQ} = 5.4$ V, $V_{IL} = 1.35$ V and $Z_0 = 50$ ohms,

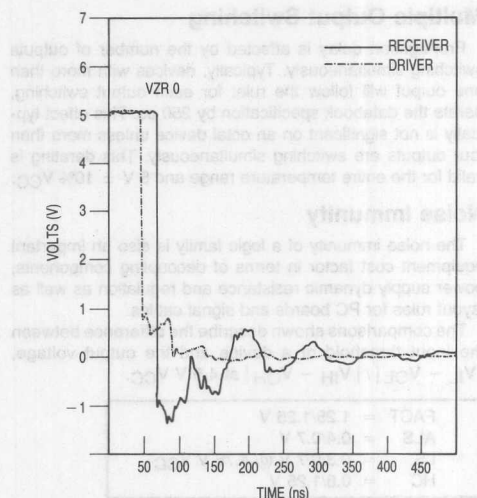


Figure 2-3d. Resultant Waveforms Driving 50 Ohm Line — Actual

I_{OL} is 75 mA at 1.65 V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 ohms, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IH} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

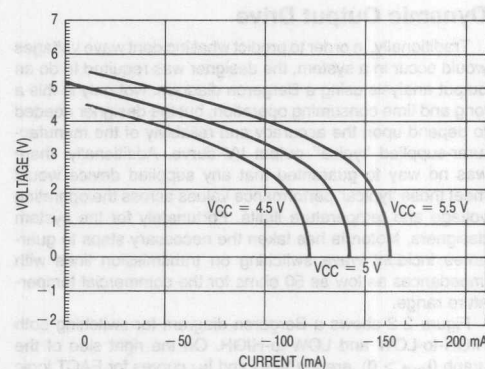


Figure 2-4. Output Characteristics V_{OH}/I_{OH} , 'AC00

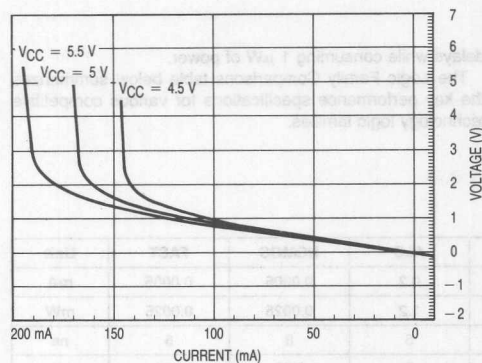


Figure 2-5. Output Characteristics V_{OL}/I_{OL} . 'AC00

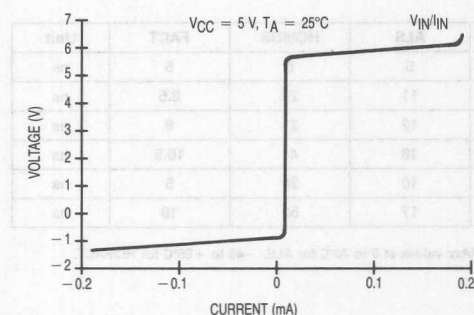


Figure 2-6. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at $3.3 \text{ V} \pm 0.3 \text{ V}$. To this end, Motorola guarantees all of its devices operational at $3.3 \text{ V} \pm 0.3 \text{ V}$. Note also that AC and DC specifications are guaranteed between 3 and 5.5 V. Operation of FACT logic is also guaranteed from 2 to 6 V on V_{CC} .

Operating Voltage Ranges

FACT	= 2 to 6 V
ALS	= $5 \text{ V} \pm 10\%$
LS	= $5 \text{ V} \pm 5\%$
HC	= 2 to 6 V

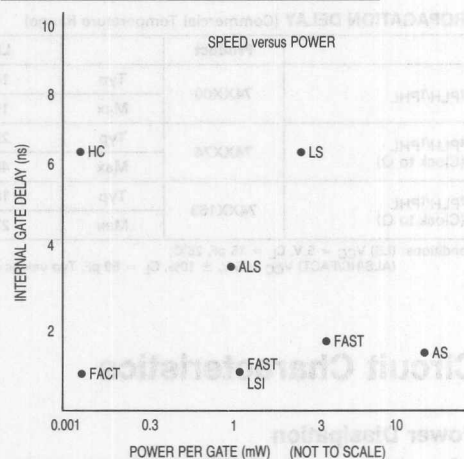


Figure 2-7. Internal Gate Delays

Figure 2-8. Logic Family Comparisons

GENERAL CHARACTERISTICS (All Max Ratings)

Symbol	Parameter	LS	ALS	HCMOS	FACT		Unit
					'AC	'ACT	
$V_{CC}/E_{E}/DD$	Operating Voltage Range	$5 \pm 5\%$	$5 \pm 10\%$	2 to 6	2 to 6	2 to 6	V
T_A 74 Series	Operating Temperature Range	0 to +70	0 to +70	-40 to +85	-40 to +85	-40 to +85	°C
V_{IH} (min)	Input Voltage (limits)	2	2	3.15	3.15	2	V
V_{IL} (max)		0.8	0.8	0.9	1.35	0.8	V
V_{OH} (min)	Output Voltage (limits)	2.7	2.7	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
V_{OL} (max)		0.5	0.5	0.1	0.1	0.1	V
I_{IH}	Input Current	20	20	+1	+1	+1	μA
I_{IL}		-400	-200	-1	-1	-1	μA
I_{OH}	Output Current at V_O (limit)	-0.4	-0.4	-4 @ $V_{CC} - 0.8$	-24 @ $V_{CC} - 0.8$	-24 @ $V_{CC} - 0.8$	mA
I_{OL}		8	8	4 @ 0.4 V	24 @ 0.4 V	24 @ 0.4 V	mA
DCM	DC Noise Margin LOW/HIGH	0.3/0.7	0.4/0.7	0.8/1.25	1.25/1.25	0.7/2.4	V

Note: All DC parameters are specified over the commercial temperature range.

FACT DATA

FACT Replaces LS, ALS, HCMOS

Motorola's Advanced CMOS family is specifically designed to outperform the LS, ALS and HCMOS families. Figure 2-7 shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation

delays while consuming 1 μ W of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

Figure 2-8. Logic Family Comparisons, cont'd.

SPEED/POWER CHARACTERISTICS (All Typical Ratings)

Symbol	Parameter	LS	ALS	HCMOS	FACT	Unit
I_G	Quiescent Supply Current/Gate	0.4	0.2	0.0005	0.0005	mA
P_G	Power/Gate (Quiescent)	2	1.2	0.0025	0.0025	mW
t_p	Propagation Delay	7	5	8	5	ns
—	Speed Power Product	14	6	0.02	0.01	pJ
f_{max}	Clock Frequency D/FF	33	50	50	160	MHz

PROPAGATION DELAY (Commercial Temperature Range)

	Product		LS	ALS	HCMOS	FACT	Unit
t_{PLH}/t_{PHL}	74XX00	Typ	10	5	8	5	ns
		Max	15	11	23	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	25	12	23	8	ns
		Max	40	18	44	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	18	10	20	5	ns
		Max	27	17	52	10	ns

Conditions: (LS) $V_{CC} = 5$ V, $C_L = 15$ pF, 25°C;
(ALS/HC/FACT) $V_{CC} = 5$ V, $\pm 10\%$, $C_L = 50$ pF, Typ values at 25°C, Max values at 0 to 70°C for ALS, -40 to +85°C for HC/FACT.

Circuit Characteristics

Power Dissipation

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Power consumption of a circuit can be calculated using the formula:

$$P_D = [(C_L + C_{PD}) \cdot V_{CC} \cdot V_S \cdot f] + [I_Q \cdot V_{CC}]$$

where

P_D = power dissipation (W)

C_L = load capacitance (Farad)

C_{PD} = device power capacitance (Farad)

V_{CC} = power supply (Volt)

V_S = output voltage swing (Volt)

f = frequency of operation (Hz)

I_Q = quiescent current (Amp)

Power consumption for FACT is dependent on the supply voltage, frequency of operation, internal capacitance and load. V_S will be V_{CC} and I_Q can be considered negligible for CMOS. Therefore, the simplified formula for CMOS is:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

C_{PD} values for CMOS devices are calculated by measuring the power consumption of a device at two different frequencies. C_{PD} is calculated in the following manner:

1. The power supply voltage is set to $V_{CC} = 5$ Vdc.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst-case situation per JEDEC C_{PD} conditions (see Section 3).

3. The power supply current is measured and recorded at input frequencies of 200 kHz and 1 MHz.

4. The power dissipation capacitance is calculated by solving the two simultaneous equations

$$P_1 = (C_{PD} \cdot V_{CC}^2 \cdot f_1) + (I_{CC} \cdot V_{CC})$$

$$P_2 = (C_{PD} \cdot V_{CC}^2 \cdot f_2) + (I_{CC} \cdot V_{CC})$$

giving

$$C_{PD} = (P_1 - P_2) / V_{CC}^2 (f_1 - f_2)$$

or

$$C_{PD} = (I_1 - I_2) / V_{CC} (f_1 - f_2)$$

where

I_1 = supply current at $f_1 = 200$ kHz.

I_2 = supply current at $f_2 = 1$ MHz.

On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual device function, if there is more than one (i.e., gates, flip-flops, etc.), within the package.

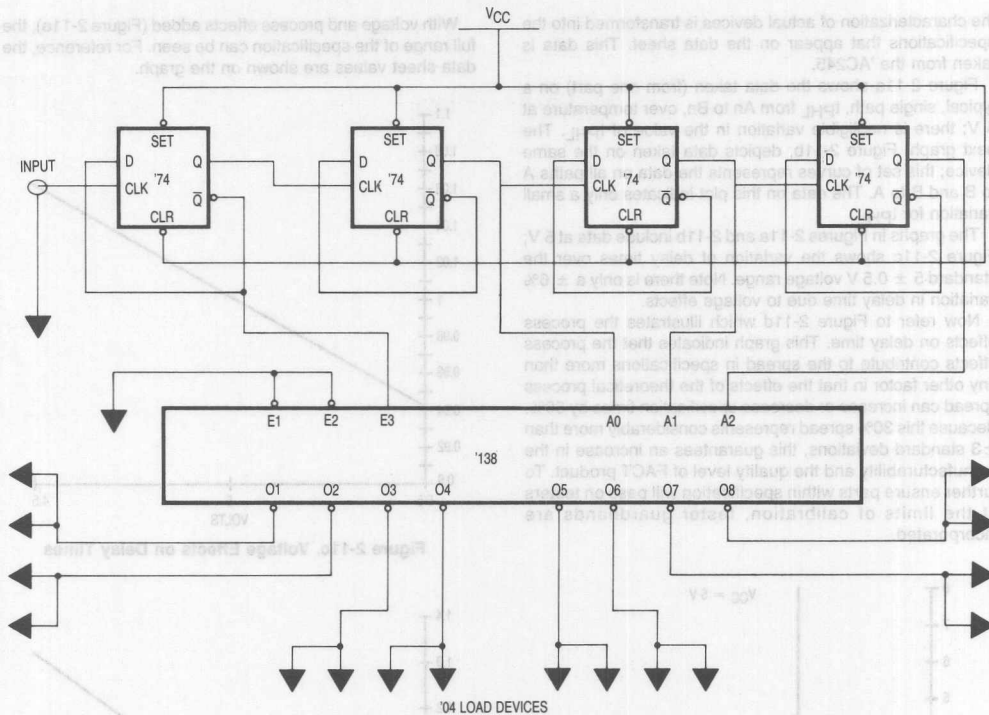


Figure 2-9. Power Demonstration Circuit Schematic

The circuit shown in Figure 2-9 was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a '138 decoder. This generated eight

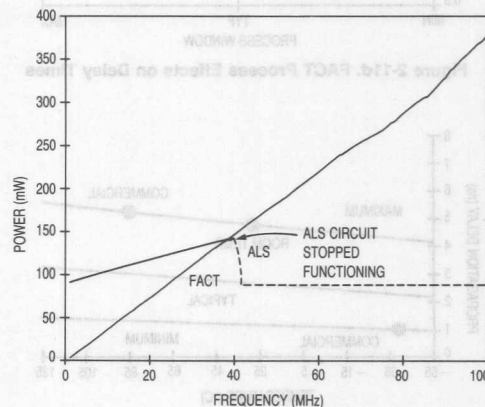


Figure 2-10. FACT versus ALS Circuit Power

non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. Figure 2-10 illustrates the results of these measurements.

Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to near zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities above 40 MHz. At this frequency, the first 74ALS74 D-type flip-flop ceased to operate. Once this occurred, the entire circuit stopped working and the power consumption fell to its quiescent value. The FACT device, however, continued functioning beyond the limit of the frequency generator, which was 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

Refer to Section 3 for test philosophies regarding power dissipation.

Specification Derivation

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 2-11a through 2-11e illustrate how the data from

the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'AC245.

Figure 2-11a shows the data taken (from one part) on a typical, single path, t_{PHL} from An to Bn, over temperature at 5 V; there is negligible variation in the value of t_{PHL} . The next graph, Figure 2-11b, depicts data taken on the same device; this set of curves represents the data on all paths A to B and B to A. The data on this plot indicates only a small variation for t_{PHL} .

The graphs in Figures 2-11a and 2-11b include data at 5 V; Figure 2-11c shows the variation of delay times over the standard 5 ± 0.5 V voltage range. Note there is only a $\pm 6\%$ variation in delay time due to voltage effects.

Now refer to Figure 2-11d which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ± 3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

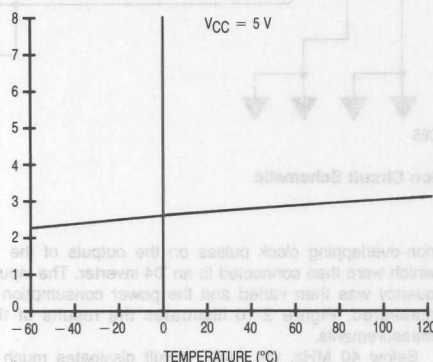


Figure 2-11a. t_{PHL} , An to Bn, Single Path

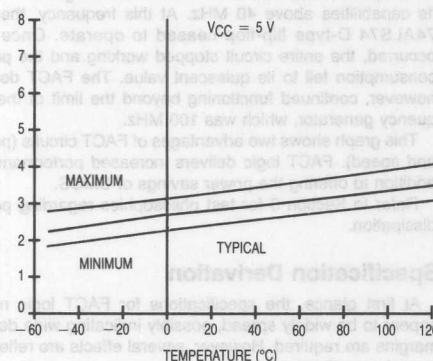


Figure 2-11b. t_{PHL} , A to B, All Paths

With voltage and process effects added (Figure 2-11e), the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

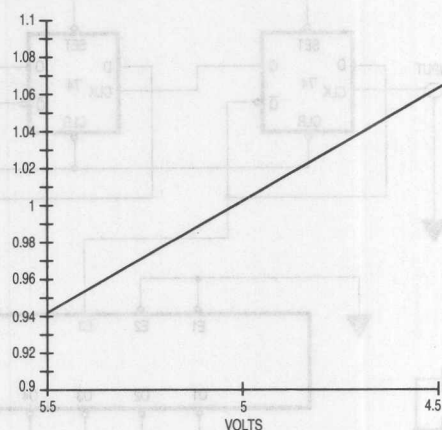


Figure 2-11c. Voltage Effects on Delay Times

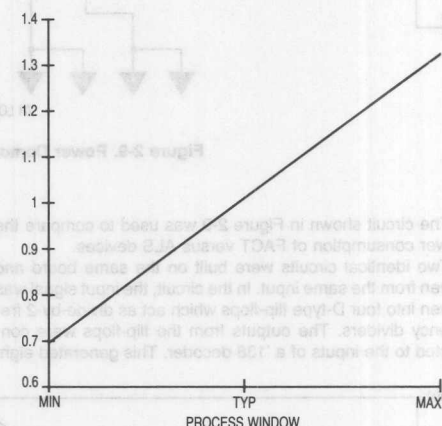


Figure 2-11d. FACT Process Effects on Delay Times

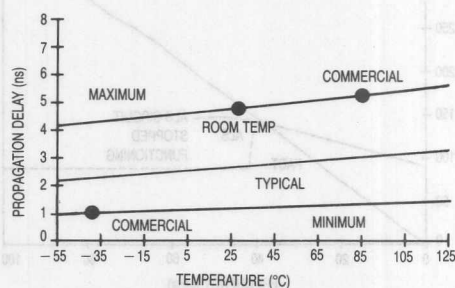


Figure 2-11e. t_{PHL} , A to B, with Voltage and Process Variation

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3 ns while the hold time is 0 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5 V, the setup time is 1.5 ns while the hold time is -1.5 ns. They are the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true 'critical' time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (3 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

Capacitive Loading Effects

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delays are measured to the 50% point of the output waveform.

Parameter	Voltage (V)			Units
	3	4.5	5.5	
t_{rise}	31	22	19	ps/pF
t_{fall}	18	13	12.5	ps/pF

$T_A = 25^\circ\text{C}$

The two graphs following, Figures 2-12 and 2-13, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). Figures 2-14 and 2-15 show the effects of lumped load capacitance on rise and fall times for FACT devices.

Latch-up

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions ($T_A = 125^\circ\text{C}$ and $V_{CC} = 5.5\text{ Vdc}$). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

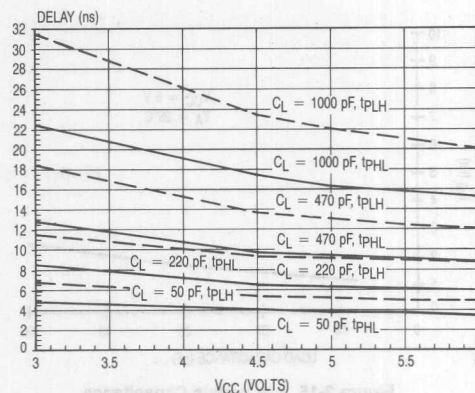


Figure 2-12. Propagation Delay versus V_{CC} ('AC00)

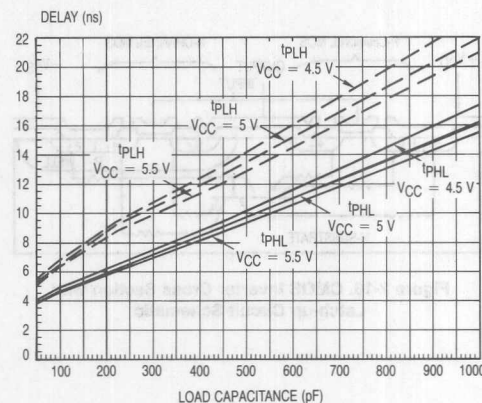


Figure 2-13. Propagation Delay versus C_L ('AC00)

FACT devices have been specifically designed to reduce the possibility of latch-up occurring; Motorola accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

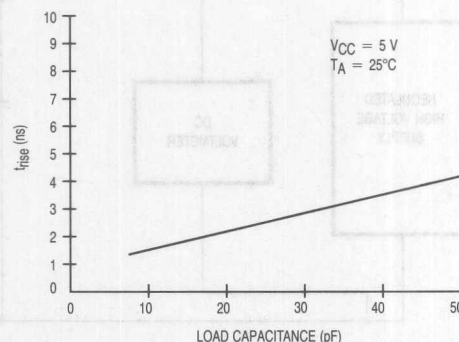


Figure 2.14. t_{rise} versus Capacitance

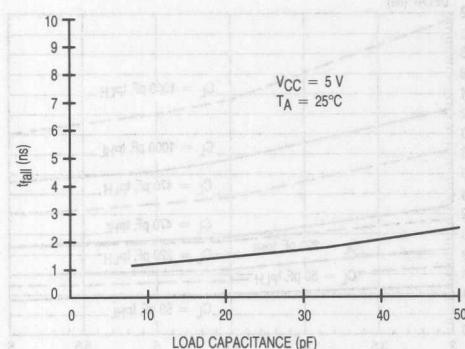
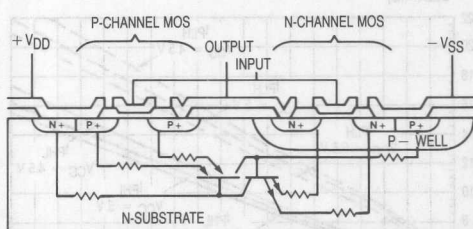
Figure 2-15. t_{fall} versus Capacitance

Figure 2-16. CMOS Inverter Cross Section with Latch-up Circuit Schematic

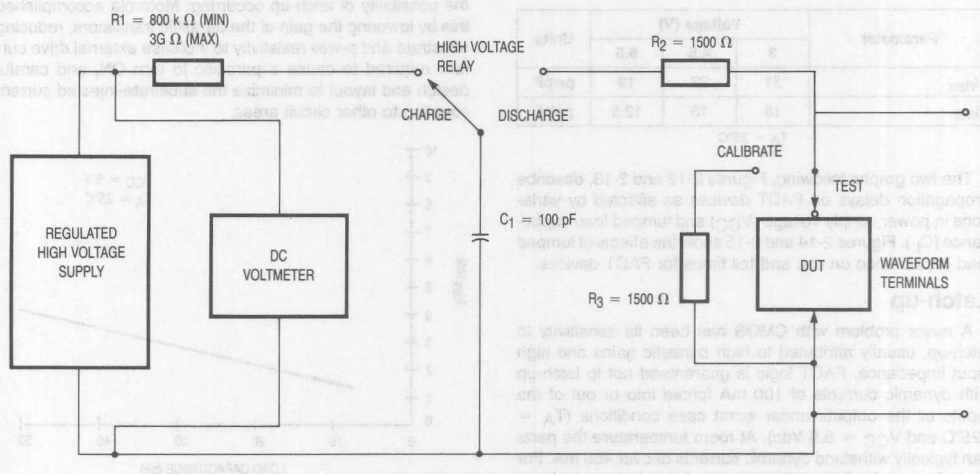


Figure 2-17. ESD Test Circuit

Electrostatic Discharge (ESD) Sensitivity

FACT circuits show excellent resistance to ESD-type damage. FACT logic is guaranteed to have 2000 V ESD immunity on all inputs and outputs using Human Body Model (1500 ohms, 100 pF). FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 2-17 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 2-18 is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows: five pulses, each of 2000 V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. The voltage is increased and the testing procedure is again performed; this entire process is repeated until failure is detected. This is done to thoroughly evaluate all pins.

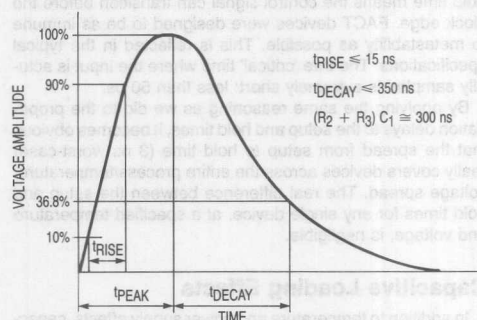


Figure 2-18. ESD Pulse Waveform

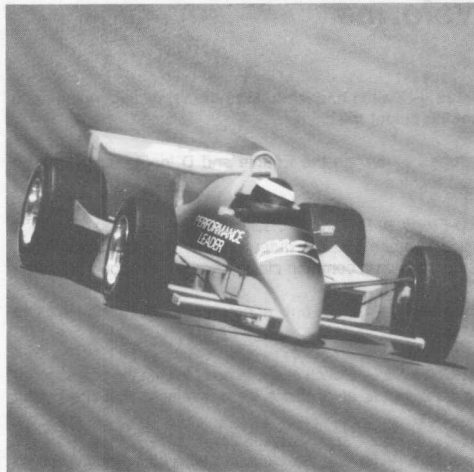


FIGURE 1. A Formula 1 race car.

Shift Registers — Switch the clock pin with other inputs. Disconnected such that the device counts.

Transceivers — Switch one data input. For bidirectional devices enable only one direction.

Parity Generator — Switch one input.

Priority Encoder — Switch the lowest priority input.

Load Capacitance — Each output which is switching should be loaded with the standard 50 pF.

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz, the following formula can be used to calculate C_{DP}:

$$C_{DP} = 100(V_{CC}/f) \times 10^9 \text{ — Equivalent Load Capacitance}$$

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +1.8	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current, per Pin	±50	nA
I _{OUT}	DC Output Current, per Pin	±50	nA
I _{CC}	DC V _{CC} or GND Current, per Output Pin	±50	nA
T _{STG}	Storage Temperature	-55 to +150	°C

FIGURE 2. Absolute Maximum Ratings. The values in this table are the maximum values which the device can handle without exceeding the maximum ratings. Exceeding the maximum ratings may cause permanent damage to the device. The values in this table are the maximum values which the device can handle without exceeding the maximum ratings. Exceeding the maximum ratings may cause permanent damage to the device.

Ratings, Specifications and Waveforms

Specifying FACT Devices

Traditionally, when a semiconductor manufacturer designs a new device for introduction, specifications were based on the characteristics of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual behavior of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. Motorola tested and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specifications, Motorola devised a systematic and thorough process to generate specifications. Devices are selected from multiple lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits.

The method of characterizing parts more accurately represents the product across time, voltage, temperature, and process rather than portraying the fastest possible device.

FACT specifies a test method for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with V_{CC} = 5 V at 25°C, with 50-ohm output pins enabled and disabled.

Power Dissipation — Test Philosophy

In an effort to reduce confusion about measuring C_{DP}, a JEDEC standard test procedure (Jepc-504) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with V_{CC} = 5 V at 25°C, with 50-ohm output pins enabled and disabled.

Ratings and Specifications

FIGURE 3-1. Absolute Maximum Ratings.

Ratings, Specifications and Waveforms

Specifying FACT Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

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To provide more realistic and manufacturable specs, Motorola devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device. FACT circuits are therefore guaranteed to be manufacturable over time without the need to respecify timing.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation — Test Philosophy

In an effort to reduce confusion about measuring C_{PD} , a JEDEC standard test procedure (Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with $V_{CC} = 5\text{ V}$ at 25°C , with 3-state outputs both enabled and disabled.

Gates — Switch one input. Bias the remaining inputs such that the output switches.

Latches — Switch the Enable and D inputs such that the latch toggles.

Flip-Flops — Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.

Decoders — Switch one address pin which changes two outputs.

Multiplexers — Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.

Counters — Switch the clock pin with other inputs biased such that the device counts.

Shift Registers — Switch the clock pin with other inputs biased such that the device counts.

Transceivers — Switch one data input. For bidirectional devices enable only one direction.

Parity Generator — Switch one input.

Priority Encoders — Switch the lowest priority input.

Load Capacitance — Each output which is switching should be loaded with the standard 50 pF.

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz, the following formula can be used to calculate C_{PD} :

$$C_{PD} = I_{CC}/(V_{CC}) (1 \times 10^6) - \text{Equivalent Load Capacitance}$$

Ratings and Specifications

Figure 3-1. Absolute Maximum Ratings¹

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Source/Sink Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$

¹Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Motorola does not recommend operation of FACT circuits outside databook specifications.

Figure 3-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
		4.5	5.0	5.5	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = - 40°C to + 85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = - 50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} - 24 mA - 24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			- 75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

*All outputs loaded; thresholds on input associated with output under test.



capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in average applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

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The 500 ohm resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500 ohm resistor to ground can simply be a 450 ohm resistor feeding into a 50 ohm coaxial cable leading to a sampling scope input connector, with the internal 50 ohm termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See Figure 3-3.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also

serves as a 50 ohm termination for the pulse generator that supplies the input signal.

Shown in Figure 3-3 is a second 500 ohm resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-state output. With the switch closed, the pair of 500 ohm resistors and the $2 \times V_{CC}$ supply voltage establish a quiescent HIGH level.

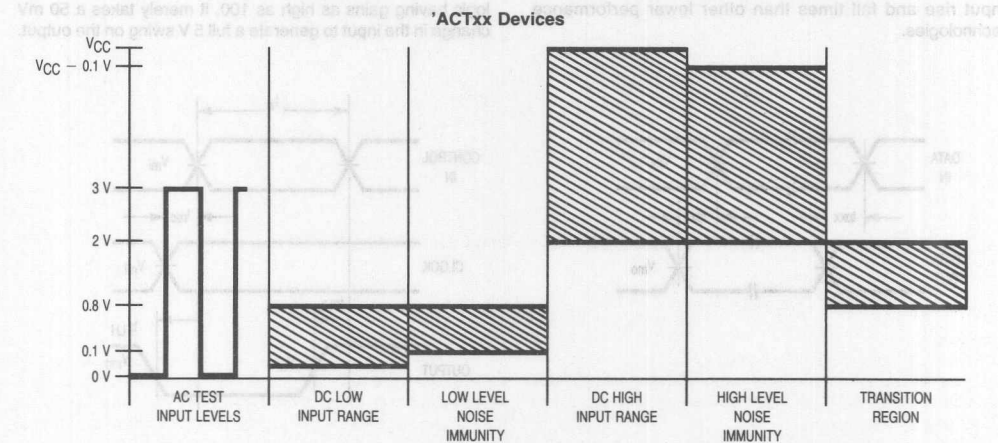
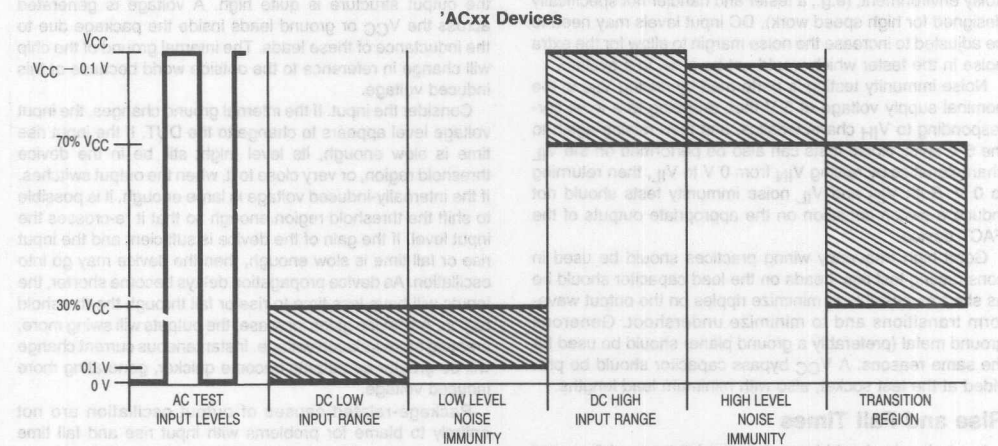


Figure 3-4b. Test Input Signal Levels

Test Conditions

Figures 3-4a and 3-4b describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0 V for a logic LOW to 3 V for a logic HIGH for 'ACT devices and 0 V to V_{CC} for 'AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5 V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 5 V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL} , then returning to 0 V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3 ns and signal swing of 0 V to 3.0 V V_{CC} for 'ACT devices or 0 V to V_{CC} for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

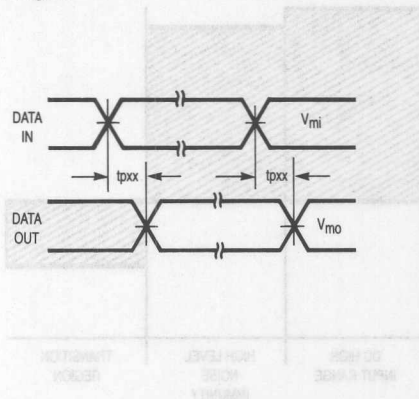


Figure 3-5. Waveform for Inverting and Non-Inverting Functions

V_{mi} = 50% V_{CC} for 'AC devices; 1.5 V for 'ACT devices
 V_{m0} = 50% for 'AC/'ACT devices

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{CC} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it re-crosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{CC} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5 V swing on the output.

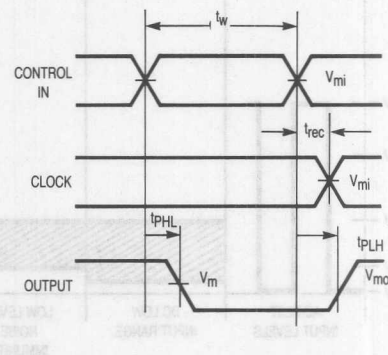


Figure 3-6. Propagation Delay, Pulse Width and t_{rec} Waveforms

Enable and Disable Times

Figures 3-8 and 3-9 show that the disable times are measured at the point where the output voltage has risen or fallen by 10% from the voltage rail level (i.e., ground for t_{PLZ} or V_{CC} for t_{PHZ}). This change enhances the repeatability of measurements, reduces test times, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 10% of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 10% is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable time and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

Propagation Delay, f_{max} , Set, Hold, and Recovery Times

A 1 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max} . A 50% duty cycle should always be used when testing f_{max} . Two pulse generators are usually required for testing such parameters as setup time (t_s), hold time (t_h), recovery time (t_{rec}) shown in Figure 9.

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

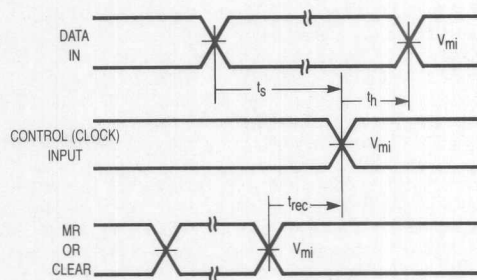


Figure 3-7. Setup Time, Hold Time and Recovery Time

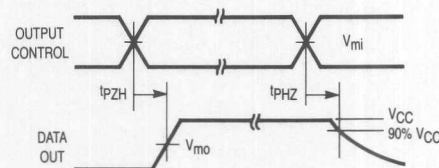


Figure 3-8. 3-State Output High Enable and Disable Times

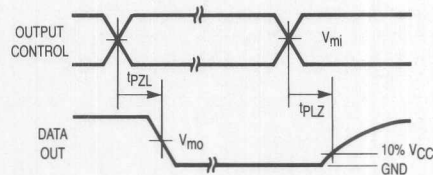


Figure 3-9. 3-State Output Low Enable and Disable Times

* V_{mi} = 50% V_{CC} for 'AC' devices; 1.5 V for 'ACT' devices
 V_{m0} = 50% V_{CC} for 'AC'/'ACT' devices

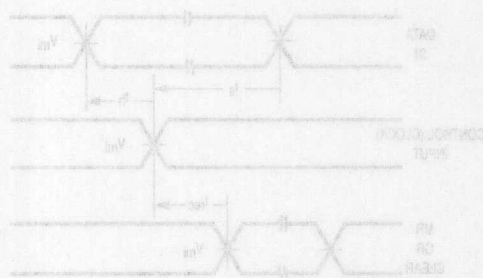


Figure 3-7: Setup Time, Hold Time and Recovery Time



Figure 3-8: 3-State Output High Enable and Disable Times



Figure 3-9: 3-State Output Low Enable and Disable Times

$V_{oh} = 50\% V_{CC}$ for AC devices; 1.5 V for FACT devices
 $V_{ol} = 50\% V_{CC}$ for AC/FACT devices

Enable and Disable Times

Figures 3-7 and 3-8 show that the enable times are measured at a point where the output voltage has risen or fallen by 10% from the voltage rail level (i.e., ground for V_{OL} or V_{CC} for V_{OH}). This charge enhances the repeatability of measurements, reduces test time, and gives the system designer more reliable delay times to use in calculating minimum cycle times. Since the high impedance state during a falling waveform is RC controlled, the first 10% of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 10% is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent. Disable time and thus handles system performance since the designer must use the Enable and Disable times to device wait times before signals to ensure that the output of one device is disabled before that of another device is enabled.

Propagation Delay, t_{max} , Set, Hold, and Recovery Times

A 1 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing logic. A 50% duty cycle should always be used when testing t_{max} . Two pulse generators are usually required for testing such parameters as setup time (t_s), hold time (t_h), recovery time (t_{rec}) shown in Figure 3.

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulating surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or equipment. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the test, which are near the device, are conductive and connected to ground.

Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Motorola's Advanced CMOS helps designers achieve these goals.

FACT logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high-in-out, low input loading and a 50 ohm transmission line drive capability (comparable to Motorola's FAST bipolar technology family) to offer a complete family of sub-2-micron 851 and 861 devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- **Thermal Management** — Circuit performance and long-term circuit reliability are affected by the temperature.
- **Interfacing** — Interboard and technology interface, battery backup and power down or live interconnect systems require some special thought.
- **Transmission Line Driving** — FACT has the driving capability superior to all CMOS families and most TTL families.

Design Considerations

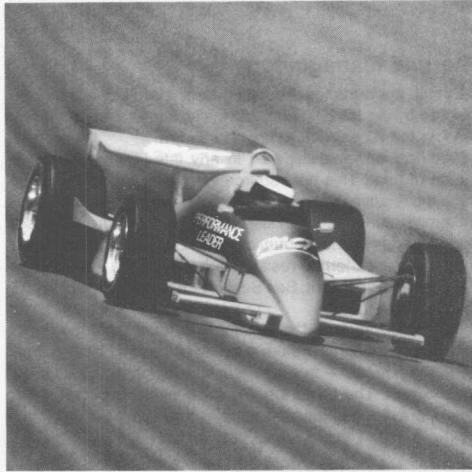
4

- **Enhanced noise immunity and high threshold levels** improve FACT's resistance to external problems.
- **Board layout** — Product board layout will analyze that most noise effects are minimized.
- **Power Supplies and Decoupling** — Maximize ground and VCC traces to keep VCC/ground impedance as low as possible. Full ground/VCC planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.

Figure 4-1. Thermal Resistance Values for Standard IC Packages

Thermal Resistance in Still Air						
Package Description						
No. Leads	Body Style	Body Material	Body W x L	Die Bond	Die Area (sq mils)	Pad Area (sq mils)
14	DL	Epoxy	174 x 344	Epoxy	4096	6100
16	DL	Epoxy	174 x 344	Epoxy	4096	12100
20	DL	Epoxy	174 x 344	Epoxy	4096	14400
NOTE: 1. All plastic packages use copper lead frames. 2. Body style DL is "Dust-In-Line". 3. Standard mounting method: Dust-In-Line socket or P/D board with no contact between bottom of package and socket or P/D board.						
Thermal Resistance in Still Air						
Package Description						
No. Leads	Body Style	Body Material	Body W x L	Die Bond	Die Area (sq mils)	Pad Area (sq mils)
14	DL	Epoxy	174 x 344	Epoxy	4096	6100
16	DL	Epoxy	174 x 344	Epoxy	4096	12100
20	DL	Epoxy	174 x 344	Epoxy	4096	14400

FACT DATA



where
 $T_J = T_A + P_D \theta_{JA}$
 T_J = maximum junction temperature
 T_A = maximum ambient temperature
 P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III)
 θ_{JC} = average thermal resistance, junction to case
 θ_{CA} = average thermal resistance, case to ambient
 θ_{JA} = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and GSEC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (LAM) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature and the device case-to-ambient thermal resistance, θ_{JA} . (To some extent the device power dissipation can also be controlled, but under recommended use the VCC supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the θ_{JA} thermal resistance term. θ_{JA} is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Motorola's Advanced CMOS helps designers achieve these goals.

FACT logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50 ohm transmission line drive capability (comparable to Motorola's FAST bipolar technology family) to offer a complete family of sub 2-micron SSI and MSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- Thermal Management — circuit performance and long-term circuit reliability are affected by die temperature.
- Interfacing — interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving — FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects — As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board Layout — Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling — Maximize ground and V_{CC} traces to keep V_{CC} /ground impedance as low as possible; full ground/ V_{CC} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.

Thermal Management

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. See Section 2 for calculation of FACT power consumption.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\bar{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\bar{\theta}_{JC}$ = average thermal resistance, junction to case

$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient

$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can also be controlled, but under recommended use the V_{CC} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Figure 4-1. Thermal Resistance Values for Standard I/C Packages

Thermal Resistance in Still Air								
Package Description								
No. Leads	Body Style	Body Material	Body W x L	Die Bonds	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	θ_{JC} (°C/Watt)	
							Avg.	Max.
14	DIL	Epoxy	1/4" x 3/4"	Epoxy	4096	6,400	38	61
16	DIL	Epoxy	1/4" x 3/4"	Epoxy	4096	12,100	34	54
20	DIL	Epoxy	0.35" x 0.35"	Epoxy	4096	14,400	N/A	N/A

NOTES:

1. All plastic packages use copper lead frames.
2. Body style DIL is "Dual-In-Line."
3. Standard Mounting Method: Dual-In-Line Socket or P/C board with no contact between bottom of package and socket or P/C board.

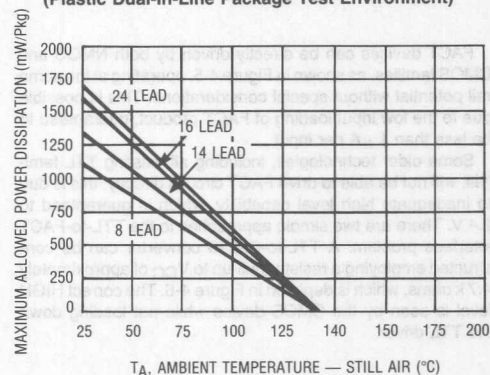
For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average $\bar{\theta}_{JC}$ resistance values for standard IC packages are given in Figure 4-1. In Figure 4-2, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geq 100,000$ hours for ceramic packages).

Figure 4-2. Ambient Temperature Derating Curves (Plastic Dual-In-Line Package Test Environment)



Air Flow

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) reduces the temperature rise of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 4-3 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each

device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

Figure 4-3. Thermal Gradient of Junction Temperature (16-Pin Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfm along the Z axis.

Optimizing The Long Term Reliability of Plastic Packages

Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1) T = (6.376 \times 10^{-9}) e^{\left[\frac{11554.267}{273.15 + T_J} \right]}$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$(2) T_J = T_A + P_D \theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on-chip power dissipation.

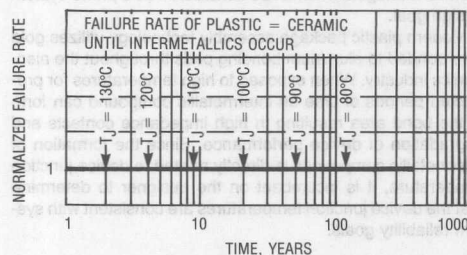
Table 1 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

TABLE 1 — DEVICE JUNCTION TEMPERATURE versus TIME TO 0.1% BOND FAILURES.

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 1 is graphically illustrated in Figure 4-4 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.

Figure 4-4. Failure Rate versus Time Junction Temperature



Procedure

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 1 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 4-4.

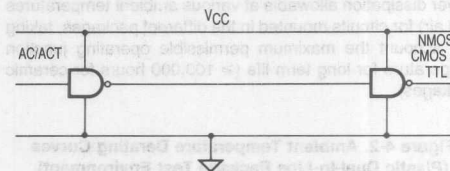
Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since $\bar{\theta}_{CA}$ is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive ALS, AS, LS, HC and HCT devices.

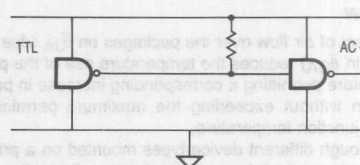
Figure 4-5. Interfacing FACT to NMOS, CMOS and TTL



FACT devices can be directly driven by both NMOS and CMOS families, as shown in Figure 4-5, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μA per input.

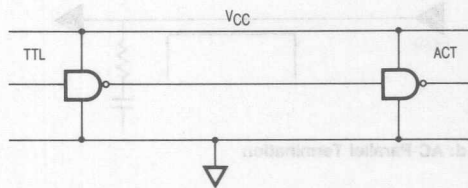
Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4 V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to V_{CC} of approximately 4.7 k ohms, which is depicted in Figure 4-6. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.

Figure 4-6. V_{IH} Pull-Up on TTL Outputs



Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, Motorola has designed devices which offer thresholds that are TTL-compatible (Figure 4-7). These interfaces tend to be slightly slower than their CMOS-level counterparts due to an extra buffer stage required for level conversion.

Figure 4-7. TTL Interfacing to 'ACT



ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to V_{CC} of approximately 4.7 k ohms). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in Figure 4-8a. Figures 4-8b and 4-8c show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.

Figure 4-8a. Resistive FACT-to-ECL Translation

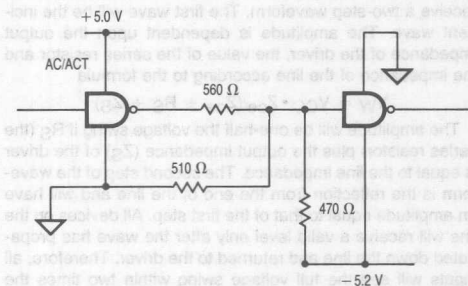


Figure 4-8b. Single-Ended ECL-to-'AC Circuit

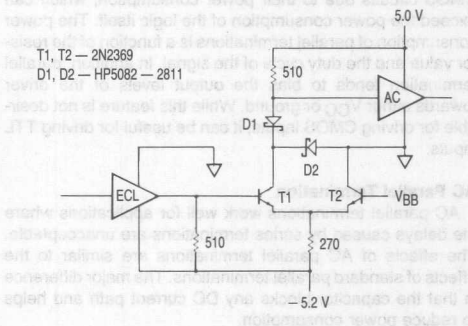
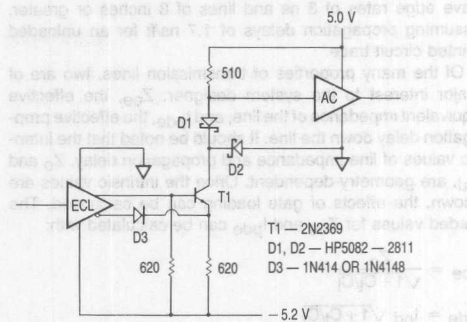
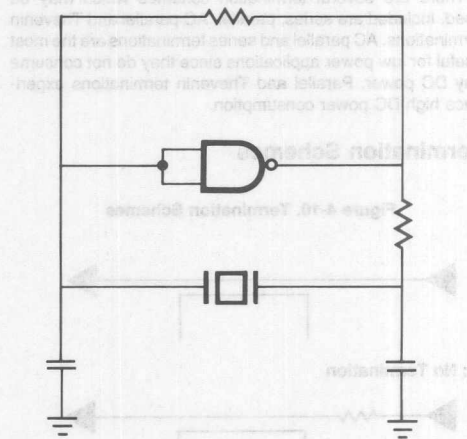


Figure 4-8c. Differential Output ECL-to-'AC Circuit



It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

Figure 4-9. Crystal Oscillator Circuit Implemented with FACT 'AC00



Line Driving

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times

properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{0e} , the effective equivalent impedance of the line, and t_{pde} , the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_0 and t_{pd} , are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{0e} and t_{pde} can be calculated with:

$$Z_{0e} = \frac{Z_0}{\sqrt{1 + C_l/C_l}}$$

$$t_{pde} = t_{pd} \sqrt{1 + C_l/C_l}$$

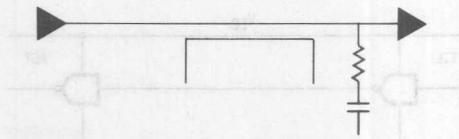
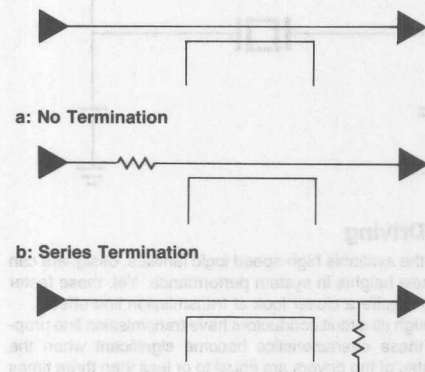
where C_l = intrinsic line capacitance and C_l = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

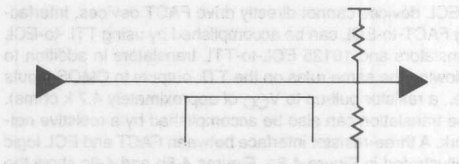
There are several termination schemes which may be used. Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Termination Schemes

Figure 4-10. Termination Schemes



d: AC Parallel Termination



e: Thevenin Termination

Series Terminations

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \cdot Z_{0e} / (Z_{0e} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

Parallel Termination

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC Parallel Termination

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination

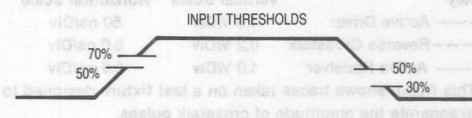
Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{CC} or ground, increasing power consumption.

FACT circuits have been designed to drive 50 ohm transmission lines over the full commercial temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on 50 ohm transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, V_{OH} and V_{OL} , are specified to be within 0.1 V of the rails, of which the output sourcing or sinking 20 μ A or less. These noise margins are outlined in Figure 4-11.

Figure 4-11. Input Threshold

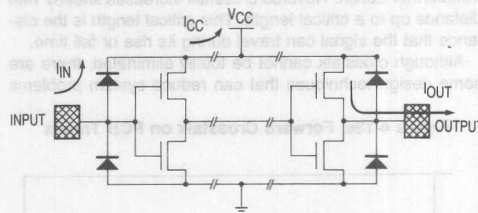


CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 4-12 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is HIGH. Depending upon the system, this current, I_{IN} , can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line.

Figure 4-12. Noise Effects



Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC} . At 5 V V_{CC} , FACT's specified input and output levels give almost 1.5 V of noise margin for both ground- and V_{CC} -born noise. With realistic input thresholds closer to 50% of V_{CC} , the actual margins approach 2.5 V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

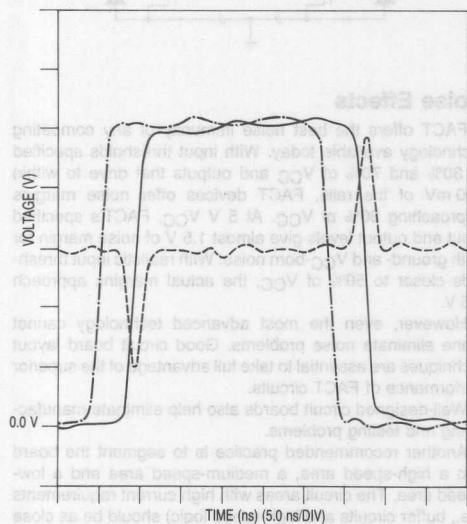
The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, Figure 4-13a, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ($\epsilon_r = 1$) and epoxy glass ($\epsilon_r = 4.7$). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figure 4-13b, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems

Figure 4-13a. Forward Crosstalk on PCB Traces

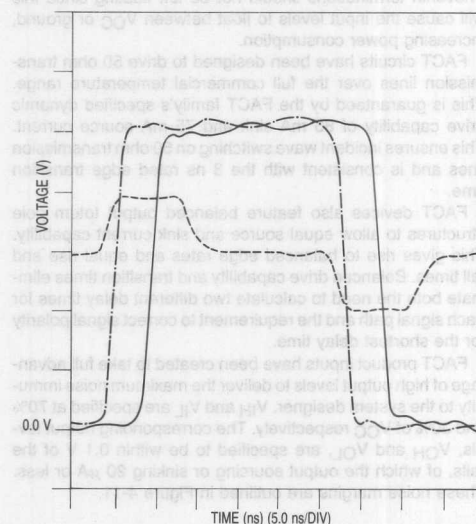


Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

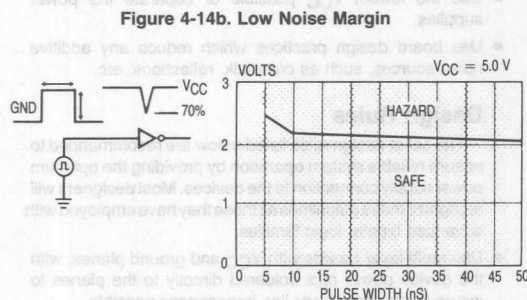
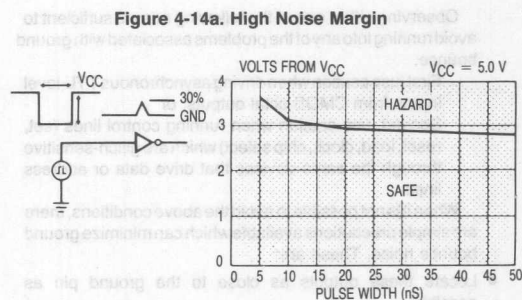
resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in Figures 4-14a and 4-14b, exemplify the outstanding immunity to everyday noise which can effect system reliability.

Figure 4-13b. Reverse Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

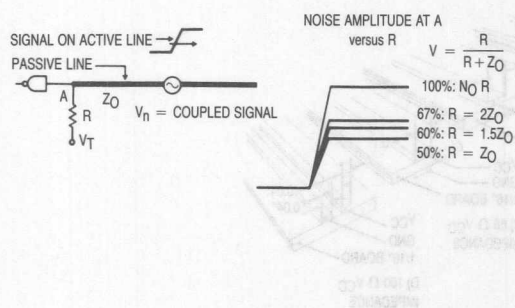
This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.



With over 2 V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

Figure 4-15. Effects of Termination on Crosstalk



Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 4-16a shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

Figure 4-16a. Output Model

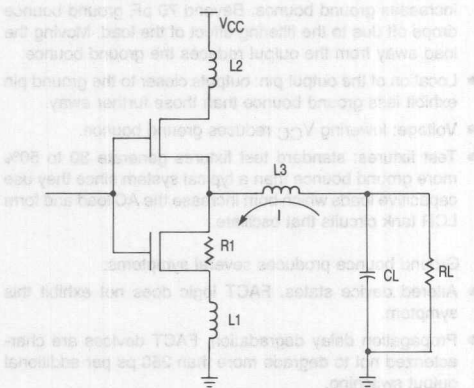


Figure 4-16b. Output Voltage

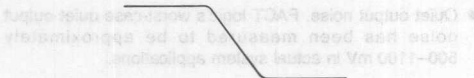
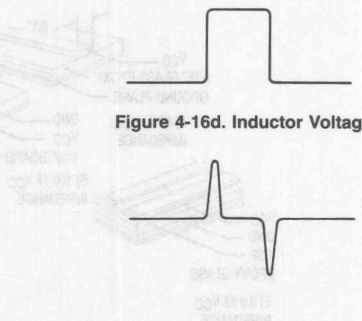


Figure 4-16c. Output Current



The three waveforms shown in Figures 4-16b, c and d, depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L , the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \cdot dV/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{gb} = -L \cdot (dI/dt)$].

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60–70 pF increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering V_{CC} reduces ground bounce.
- Test fixtures: standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are characterized not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500–1100 mV in actual system applications.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or

Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Design Rules

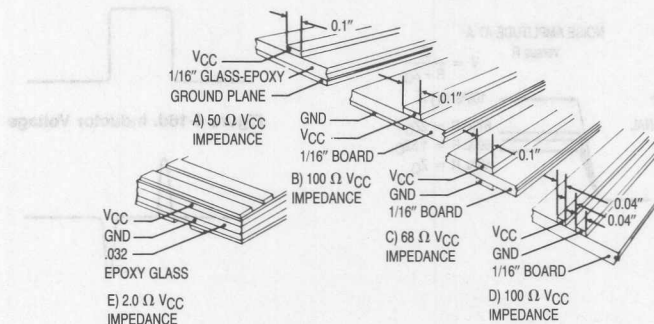
The set of design rules listed below are recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.1 μF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Do not use sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

Decoupling Requirements

Motorola Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Figure 4-17. Power Distribution Impedances

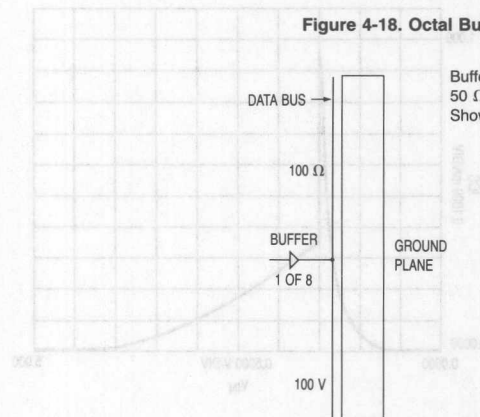


Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 4-17 displays various V_{CC} and ground layout schemes along with associated impedances.

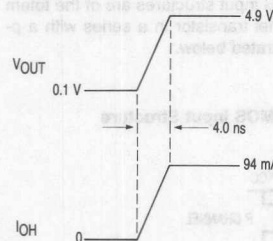
For most power distribution networks, the typical impedance is between 50 and 100 ohms. This impedance appears

in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 4-18 to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100 ohm bus from a point somewhere in the middle.

Figure 4-18. Octal Buffer Driving a 100 Ohm Bus



Buffer Output Sees Net 50 Ω Load.
50 Ω Load Line on $I_{OH}-V_{OH}$ Characteristic Shows Low-to-High Step of Approx. 4.8 V



Worst-Case Octal Drain = $8 \times 94 \text{ mA} = 0.75 \text{ Amp.}$

Being in the middle of the bus, the driver will see two 100 ohm loads in parallel, or an effective impedance of 50 ohms. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated

with the formula given in Figure 4-19.

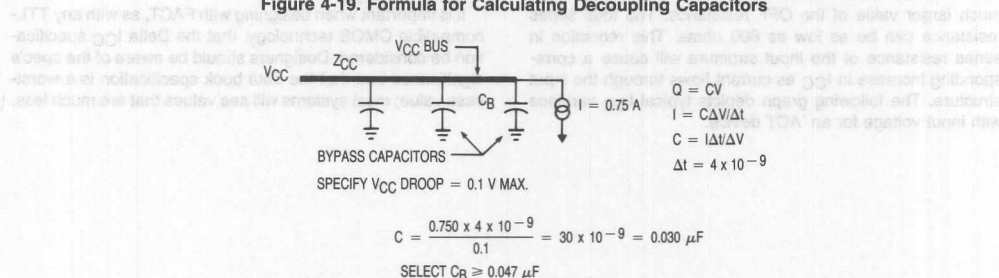
In this example, if the V_{CC} droop is to be kept below 0.1 V and the edge rate equals 4 ns, a 0.03 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Figure 4-19. Formula for Calculating Decoupling Capacitors



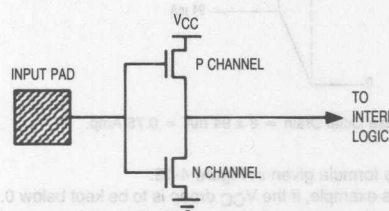
Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly throughout the logic.

TTL-Compatible CMOS Designs Require Delta I_{CC} Consideration

The FACT product line is comprised of two types of advanced CMOS circuits: 'AC and 'ACT devices. 'ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this 'ACT series is used to replace TTL, the Delta I_{CC} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

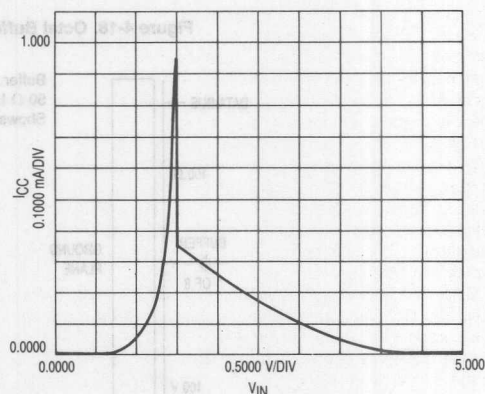
It is important to understand the concept of Delta I_{CC} and how to use it within a design. First, consider where Delta I_{CC} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.

Figure 4-20. CMOS Input Structure



These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 50 ohms while the resistance of an OFF transistor is generally greater than 5 Mohm. When the input to this structure is at either ground or V_{CC} , one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 1 μA . When the input is between ground and V_{CC} , the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600 ohms. This reduction in series resistance of the input structure will cause a corresponding increase in I_{CC} as current flows through the input structure. The following graph depicts typical I_{CC} variance with input voltage for an 'ACT device.

Figure 4-21. I_{CC} versus Input Voltage for 'ACT Devices



The Delta I_{CC} specification is the increase in I_{CC} . For each input at V_{CC} -2.1 V, the Delta I_{CC} value should be added to the quiescent supply current to arrive at the circuit's worst-case static I_{CC} value.

Fortunately, there are several factors which tend to reduce the increase in I_{CC} per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5 V. Additionally, the typical I_{CC} increase per input will be less than the specified limit. As shown in the graph above, the I_{CC} increase at V_{CC} -2.1 V is less than 200 μA in the typical system. Experiments have shown that the I_{CC} of an 'ACT240 series device typically increases only 200 μA when all of the inputs are connected to a FAST device instead of ground or V_{CC} .

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{CC} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

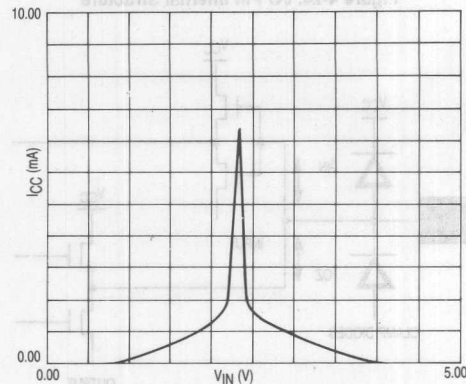
Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for I_{CC} and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{CC} specification orders of magnitude less than standard load currents. Most CMOS I_{CC} specifications are usually less than 100 μ A. When conducting an I_{CC} test, greater care must be taken so that other currents will not mask the actual I_{CC} of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{CC} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{CC} test. Even a standard 500 ohm load resistor will sink 10 mA at 5 V, which is more than twice the I_{CC} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{CC} tests.

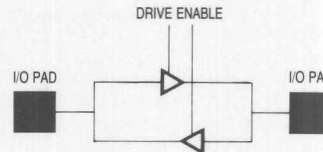
Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{CC} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from V_{CC} to ground. This conduction path leads to the increased I_{CC} current seen in the I_{CC} vs. V_{IN} curve. When the input is at either rail, the input structure no longer conducts. Most I_{CC} testing is done with all of the inputs tied to either V_{CC} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{CC} of the device under test which is being measured by the tester.

Figure 4-22. I_{CC} versus I_{IN}



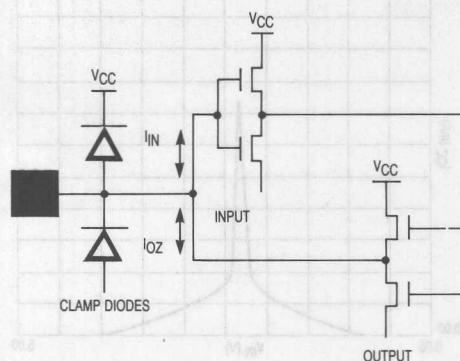
When testing the I_{CC} of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.

Figure 4-23. '245 I/O Structure



input, output and output disabled. However, only two states actually exist.

Figure 4-24. I/O Pin Internal Structure



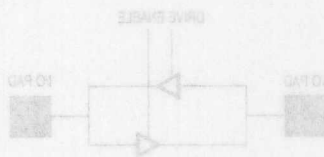
signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{CC} to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an I_{CC} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. For FACT devices, I_{IN} is specified at $\pm 1 \mu A$ while I_{OZ} is specified at $\pm 5 \mu A$. Combining these gives a limit of $\pm 6 \mu A$ for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with an understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

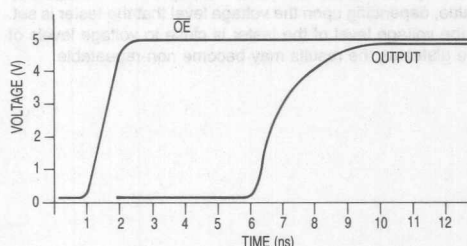
Figure 4-25. I/O Structure



Testing Disable Times of 3-State Outputs in a Transmission Line Environment

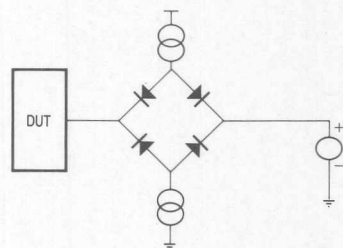
Traditionally, the disable time of a 3-state buffer has been measured from the 50% point on the disable input, to the 10% or 90% point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

Figure 4-25. Typical Bench 3-State Waveform



ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

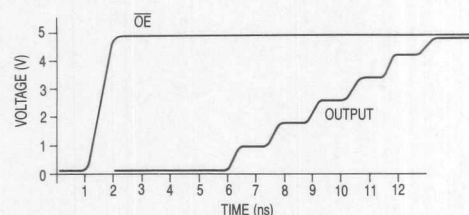
Figure 4-26. MCT Wheatstone Bridge Test Load



The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL} . When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the 10% or 90% level.

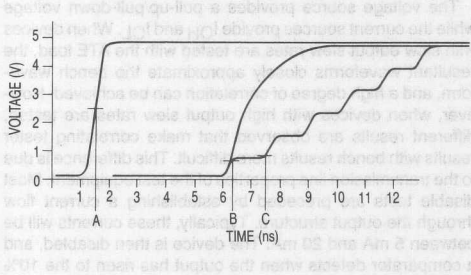
Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in Figure 4-23.

Figure 4-27. Typical ATE 3-State Waveform



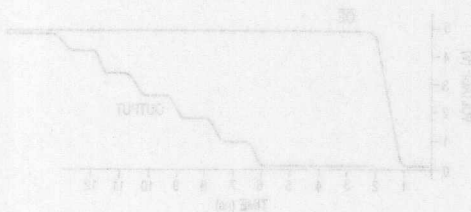
Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA

Figure 4-28. Measurement Stepout



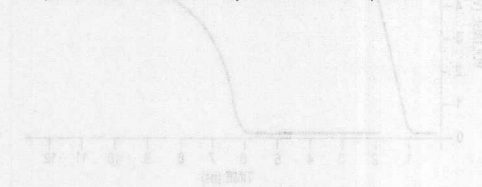
Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line and the switch is open. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance test load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the test load. At this point, the current source impedance decreases and it will dissipate its energy. A typical waveform on a modern ATE is depicted in Figure 4-29.

Figure 4-29. Typical ATE 3-State Waveform



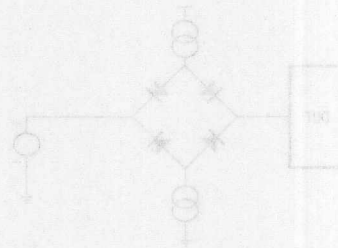
and impedances of 50 to 60 ohms, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the 10% point, it would be looking for a step of 550 mV at 5.5 V V_{CC} . Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customers' incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

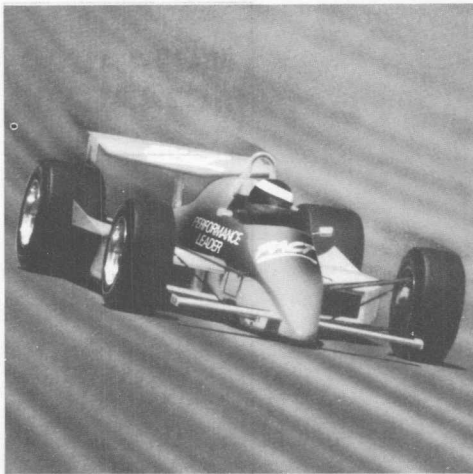
Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.



ATE test often generally are unable to duplicate the bench test results. ATE test loads often differ because they are usually not terminated away from the test device. A commonly used test load is a 50 ohm termination. The following figure illustrates the Whittaker bridge test setup that is used on the MCT 3000 test system to duplicate the bench load.

Figure 4-31. MCT Whittaker Bridge Test Load



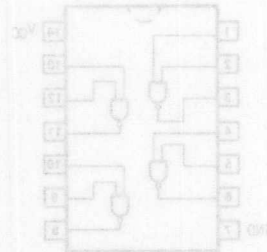


CASE 787A-82
PLASTIC
D SURF
CASE 787A-82
PLASTIC



Quad 2-Input NAND Gate

- Output Source/Sink 24 mA
- 'ACT08 Has TTL Compatible Inputs



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +1.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 50	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-55 to +150	°C

*Exceeding these ratings may cause permanent damage to the device. Functional operation should be restricted to the recommended operating conditions.

Data Sheets

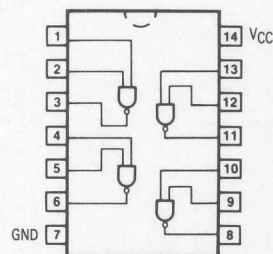


MOTOROLA

MC74AC00
MC74ACT00

Quad 2-Input NAND Gate

- Outputs Source/Sink 24 mA
- 'ACT00 Has TTL Compatible Inputs



QUAD 2-INPUT
NAND GATE



N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC00 • MC74ACT00

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} = -24 mA -24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC00 • MC74ACT00

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA -24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	2.0 1.5	7.0 6.0	9.5 8.0	2.0 1.5	10.0 8.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	5.5 4.5	8.0 6.5	1.0 1.0	8.5 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay	5.0	1.5	5.5	9.0	1.0	9.5	ns	3-5
tPHL	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

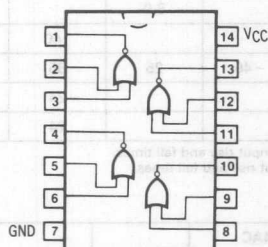
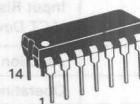
CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V

FACT DATA

**MOTOROLA****MC74AC02
MC74ACT02****Quad 2-Input NOR Gate**

- Outputs Source/Sink 24 mA
- 'ACT02 Has TTL Compatible Inputs

**QUAD 2-INPUT
NOR GATE****N SUFFIX
CASE 646-06
PLASTIC****D SUFFIX
CASE 751A-02
PLASTIC****MAXIMUM RATINGS***

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.1	0.1	0.001	0.0	Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.1	0.1	0.001	0.0	Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}
$V_{in} = V_{CC}$	$V_{out} = V_{CC}$	0.0	0.0	0.000	0.0	Maximum Low Level Output Voltage	V_{OL}

FACT DATA

MC74AC02 • MC74ACT02

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74ALS		Units	Conditions	
			T _A = +25°C		T _A = −40°C to +85°C				
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15				
		5.5	2.75	3.85	3.85				
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35				
		5.5	2.75	1.65	1.65				
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4				
		5.5	5.49	5.4	5.4				
		3.0		2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76				
		5.5		4.86	4.76				
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1				
		5.5	0.001	0.1	0.1				
			3.0		0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA
			4.5		0.36	0.44			
			5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40		μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC02 • MC74ACT02

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	5.0 4.0	7.5 6.0	1.0 1.0	8.0 6.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	5.0 4.5	7.5 6.5	1.0 1.0	8.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		8.5	1.0	9.0	ns	3-6
t _{PHL}	Propagation Delay	5.0	1.5		9.5	1.0	10	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V

FACT DATA

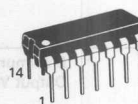
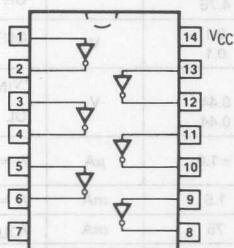


MOTOROLA

MC74AC04
MC74ACT04

Hex Inverter

- Outputs Source/Sink 24 mA
- ACT04 Has TTL Compatible Inputs



N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

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FACT DATA

MC74AC04 • MC74ACT04

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	4.5 4.0	9.0 7.0	1.0 1.0	10 7.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	4.5 3.5	8.5 6.5	1.0 1.0	9.5 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

†Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		8.5	1.0	9.0	ns	3-6
t _{PHL}	Propagation Delay	5.0	1.5		8.0	1.0	8.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V

FACT DATA

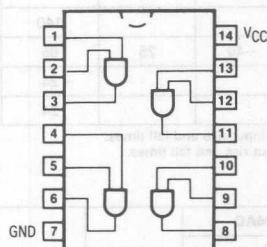


MOTOROLA

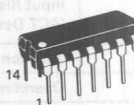
MC74AC08 MC74ACT08

Quad 2-Input AND Gate

- Outputs Source/Sink 24 mA
- 'ACT08 Has TTL Compatible Inputs



QUAD 2-INPUT AND GATE



**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	- 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC08 • MC74ACT08

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

- V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA	
		4.5		3.86	3.76		I _{OH} −24 mA	
		5.5		4.86	4.76		−24 mA	
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA	
		4.5		0.36	0.44		I _{OL} 24 mA	
		5.5		0.36	0.44		24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC08 • MC74ACT08

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = –50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA –24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	7.5 5.5	9.5 7.5	1.0 1.0	10.0 8.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	7.0 5.5	8.5 7.0	1.0 1.0	9.0 7.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC08 • MC74ACT08

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		9.0	1.0	10.0	ns	3-5
t _{PHL}	Propagation Delay	5.0	1.5		9.0	1.0	10.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	20	pF	V _{CC} = 5.0 V

V _{CC}	Supply Current	4.0	mA	V _{IN} = V _{CC} or GND
I _{OH}	Maximum Output Current	25	mA	V _{OH} = 3.5 V Min
I _{OL}	Minimum Dynamic Output Current	25	mA	V _{OL} = 1.8 V Max
I _{QTT}	Additional Max. Logic Input Leakage Current	2.5	mA	V _I = V _{CC} - 3.1 V
I _{CC}	Maximum Input Leakage Current	2.5	mA	V _I = V _{CC} or GND

*All outputs loaded with 50 pF or more. Maximum test current 10 mA and output level is 0.1 V.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.0	1.5	2.5	7.5	1.0	10.0	ns	3-5
t _{PHL}	Propagation Delay	3.0	1.5	2.5	7.5	1.0	10.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V
Voltage Range 2.5 is 2.5 V ± 0.5 V

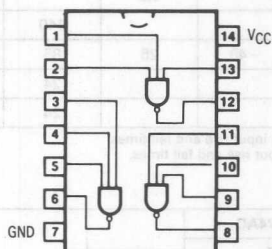


MOTOROLA

MC74AC10
MC74ACT10

Triple 3-Input NAND Gate

- Outputs Source/Sink 24 mA
- 'ACT10 Has TTL Compatible Inputs



**TRIPLE 3-INPUT
NAND GATE**

**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC10 • MC74ACT10

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74ACT		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC10 • MC74ACT10

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		5.5	1.5	2.0				
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		5.5	1.5	0.8				
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} − 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3	1.5	6.0	9.5	1.0	10.5	ns	3-5
		5.0	1.5	4.5	7.0	1.0	8.0		
t _{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.0	ns	3-5
		5.0	1.5	4.0	6.0	1.0	6.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC10 • MC74ACT10

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		9.0	1.0	10.0	ns	3-5
t _{PHL}	Propagation Delay	5.0	1.5		8.0	1.0	8.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	25	pF	V _{CC} = 5.0 V

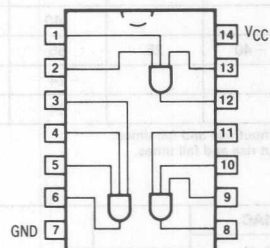


MOTOROLA

MC74AC11
MC74ACT11

Triple 3-Input AND Gate

- Outputs Source/Sink 24 mA
- 'ACT11 Has TTL Compatible Inputs



**TRIPLE 3-INPUT
AND GATE**



**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC11 • MC74ACT11

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC11 • MC74ACT11

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = − 50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			− 75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	5.5 4.0	9.5 8.0	1.0 1.0	10.0 8.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	5.5 4.0	8.5 7.0	1.0 1.0	9.5 7.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		9.5	1.0	10.5	ns	3-5
t _{PHL}	Propagation Delay	5.0	1.5		9.5	1.0	10.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	20	pF	VCC = 5.0 V

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay	3.0 2.0	1.5 1.0	2.5 4.0	9.5 8.0	1.0 1.0	10.0 8.0	ns	3-5
tPHL	Propagation Delay	3.0 2.0	1.5 1.0	2.5 4.0	9.5 7.0	1.0 1.0	8.5 7.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V



MOTOROLA

MC74AC14 MC74ACT14

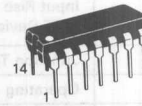
Hex Inverter Schmitt Trigger

The MC74AC14/74ACT14 contains six logic inverters which accept standard CMOS input signals (TTL levels for MC74ACT14) and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The MC74AC14/74ACT14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

- Schmitt Trigger Inputs
- Outputs Source/Sink 24 mA
- 'ACT14 Has TTL Compatible Inputs

HEX INVERTER SCHMITT TRIGGER



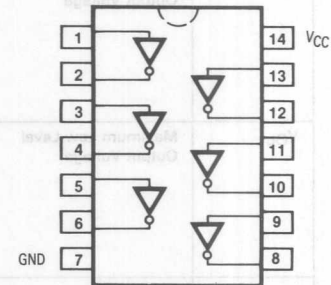
**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

FUNCTION TABLE

Input	Output
A	O
L	H
H	L



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC14 • MC74ACT14

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74ACT		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC14 • MC74ACT14

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} = −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} = 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.8		11.5	13.0	ns	3-2
t _{PLL}	Propagation Delay	5.0	1.8		10.0	11.0	ns	3-2

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pf	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	35	pf	V _{CC} = 5.0 V

MC74AC14 • MC74ACT14

INPUT CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	V _{CC} (V)	74AC Typ @ T _A = 25°C	74AC T _A = -40° to +85°C	Units	Test Conditions
V _{t+}	Maximum Positive Threshold	3.0 4.5 5.5	2.2 3.2 3.9	2.0	V	T _A = Worst Case
V _{t-}	Minimum Negative Threshold	3.0 4.5 5.5	0.5 0.9 1.1	0.8	V	T _A = Worst Case
V _{h(max)}	Maximum Hysteresis	3.0 4.5 5.5	1.2 1.4 1.6	1.2	V	T _A = Worst Case
V _{h(min)}	Minimum Hysteresis	3.0 4.5 5.5	0.3 0.4 0.5	0.4	V	T _A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC			74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay	3.3 5.0	1.5 1.5	9.5 7.0	13.5 10.0	1.5 1.5	15.0 11.0	ns	3-5
tPHL	Propagation Delay	3.3 5.0	1.5 1.5	7.5 6.0	11.5 8.5	1.5 1.5	13.0 9.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		11.5	1.0	12.5	ns	3-5
t _{PHL}	Propagation Delay	5.0	1.5		10.0	1.0	11.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

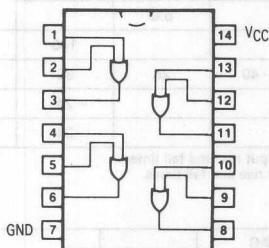
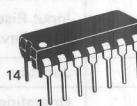
CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	25	pF	V _{CC} = 5.0 V

**MOTOROLA****MC74AC32
MC74ACT32**

Quad 2-Input OR Gate

- Outputs Source/Sink 24 mA
- 'ACT32 Has TTL Compatible Inputs

**QUAD 2-INPUT
OR GATE****N SUFFIX
CASE 646-06
PLASTIC****D SUFFIX
CASE 751A-02
PLASTIC**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC32 • MC74ACT32

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC32 • MC74ACT32

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	7.0 5.5	9.0 7.5	1.5 1.0	10.0 8.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	7.0 5.0	8.5 7.0	1.0 1.0	9.0 7.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC32 • MC74ACT32

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5		9.0	1.0	10.0	ns	3-6
t _{PHL}	Propagation Delay	5.0	1.5		9.0	1.0	10.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	20	pF	VCC = 5.0 V

ICC	Supply Current	2.5	mA	VIN = VCC or GND
IOL	Output Current	2.5	mA	VOL = 0.2 V Max
IOL	Minimum Dynamic Output Current	2.5	mA	VOL = 0.2 V Max
IOL	Additional Max. IC Output	2.5	mA	V = VCC = 2.1 V
IOH	Maximum Input Leakage Current	2.5	mA	V = VCC or GND

*All output loaded, threshold on input associated with output under test.
Maximum test duration 5 sec unless output loaded is 1 min.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT				74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF				TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Max		
tPLH	Propagation Delay	2.5	1.5	1.0	2.0	1.5	1.0	2.0	ns	3-6
tPHL	Propagation Delay	2.5	1.5	1.0	2.0	1.5	1.0	2.0	ns	3-6

Voltage Range 5.0 is 5.0 V ± 0.5 V
Voltage Range 2.0 is 2.0 V ± 0.2 V

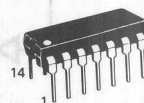
**MOTOROLA****MC74AC74
MC74ACT74****Dual D-Type Positive
Edge-Triggered Flip-Flop**

The MC74AC74/74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q , \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

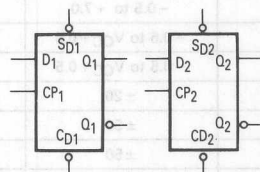
- Outputs Source/Sink 24 mA
- 'ACT74 Has TTL Compatible Inputs

**DUAL D-TYPE POSITIVE
EDGE-TRIGGERED
FLIP-FLOP**

**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

LOGIC SYMBOL**PIN NAMES**

- D_1, D_2 Data Inputs
- CP_1, CP_2 Clock Pulse Inputs
- \bar{C}_D1, \bar{C}_D2 Direct Clear Inputs
- \bar{S}_D1, \bar{S}_D2 Direct Set Inputs
- $Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$ Outputs

TRUTH TABLE (Each Half)

Inputs				Outputs	
\bar{S}_D	\bar{C}_D	CP	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	\downarrow	H	H	L
H	H	\downarrow	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

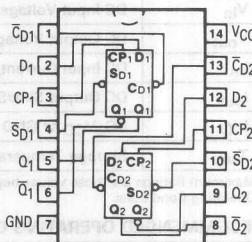
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

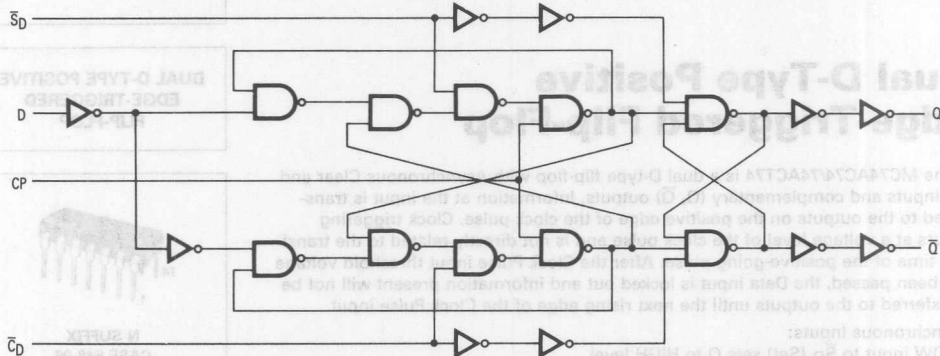
 \downarrow = LOW-to-HIGH Clock Transition $Q_0(\bar{Q}_0)$ = Previous $Q(\bar{Q})$ before

LOW-to-HIGH Transition of Clock



MC74AC74 • MC74ACT74

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	150		ns/V
		$V_{CC} @ 4.5 V$	40		
		$V_{CC} @ 5.5 V$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	10		ns/V
		$V_{CC} @ 5.5 V$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

FACT DATA

MC74AC74 • MC74ACT74

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC74 • MC74ACT74

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = – 50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} – 24 mA I _{OH} – 24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			– 75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 125		MHz	3-3
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3 5.0	5.0 3.5	8.0 6.0	12.0 9.0	4.0 3.0	13.0 10.0	ns	3-6
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	3.5 2.5	13.5 10.5	ns	3-6
t _{PLH}	Propagation Delay C _{Pn} to Q _n or Q _n	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	4.0 3.0	16.0 10.5	ns	3-6
t _{PHL}	Propagation Delay C _{Pn} to Q _n or Q _n	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	3.5 2.5	14.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC74 • MC74ACT74

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW D _n to CP _n	3.3 5.0	1.5 1.0	4.0 3.0	4.5 3.0	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP _n	3.3 5.0	−2.0 −1.5	0.5 0.5	0.5 0.5	ns	3-9	
t _w	CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	7.0 5.0	ns	3-6	
t _{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	3.3 5.0	−2.5 −2.0	0 0	0 0	ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	145	210		125		MHz	3-3
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	5.0	3.0	5.5	9.5	2.5	10.5	ns	3-6
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	5.0	3.0	6.0	10.0	3.0	11.5	ns	3-6
t _{PLH}	Propagation Delay CP _n to Q _n or Q _n	5.0	4.0	7.5	11.0	4.0	13.0	ns	3-6
t _{PHL}	Propagation Delay CP _n to Q _n or Q _n	5.0	3.5	6.0	10.0	3.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW D _n to CP _n	5.0	1.0	3.0	3.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP _n	5.0	-0.5	1.0	1.0	ns	3-9	
t _w	CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width	5.0	3.0	5.0	6.0	ns	3-6	
t _{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	5.0	-2.5	0	0	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	35	pF	V _{CC} = 5.0 V

FACT DATA

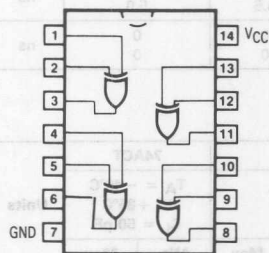


MOTOROLA

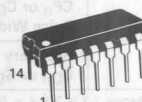
MC74AC86
MC74ACT86

Quad 2-Input Exclusive-OR Gate

- Outputs Source/Sink 24 mA



**QUAD 2-INPUT
EXCLUSIVE-OR GATE**



**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Symbol	Parameter	Typ	Max	Min
t_{pd}	Propagation Delay, V_{in} to V_{out}	1.0	3.0	0.5
t_{PHL}	High-to-Low Propagation Delay, V_{in} to V_{out}	0.5	1.0	0.2
t_{PLH}	Low-to-High Propagation Delay, V_{in} to V_{out}	0.5	1.0	0.2
t_{f}	Fall Time, V_{out} to 50% V_{CC}	0.5	1.0	0.2
t_{r}	Rise Time, V_{out} to 50% V_{CC}	0.5	1.0	0.2
t_{w}	Pulse Width	0.5	1.0	0.2
t_{rec}	Recovery Time, V_{out} to 50% V_{CC}	0.5	1.0	0.2

Symbol	Parameter	Typ	Max	Min
C_{in}	Input Capacitance	1.5	3.0	0.5
C_{pd}	Power Dissipation Capacitance	35	70	15

FACT DATA

MC74AC86 • MC74ACT86

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) *AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V V _{CC} @ 4.5 V V _{CC} @ 5.5 V	150 40 25		ns/V
t _r , t _f	Input Rise and Fall Time (Note 2) *ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V V _{CC} @ 5.5 V	10 8.0		ns/V
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC86 • MC74ACT86

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = –50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5		0.36	0.44			
I _{IIN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = –40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Inputs to Outputs	3.3 5.0	2.0 1.5	6.0 4.5	11.5 8.5	1.5 1.0	12.5 9.0	ns	3-5
t _{PHL}	Propagation Delay Inputs to Outputs	3.3 5.0	2.0 1.5	6.5 4.5	11.5 8.5	1.5 1.0	12.5 9.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5	8.5	9.5	1.0	10.0	ns	3-5
t _{PHL}	Propagation Delay	5.0	1.5	7.0	9.5	1.0	10.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	35	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

**MC74AC109
MC74ACT109**

Dual JK̄ Positive Edge-Triggered Flip-Flop

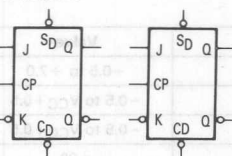
The MC74AC109/74ACT109 consists of two high-speed completely independent transition clocked JK̄ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK̄ design allows operation as a D flip-flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and K inputs together.

Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

- Outputs Source/Sink 24 mA
- 'ACT109 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

- J₁, J₂, K₁, K₂ Data Inputs
- CP₁, CP₂ Clock Pulse Inputs
- \bar{C}_D ₁, \bar{C}_D ₂ Direct Clear Inputs
- \bar{S}_D ₁, \bar{S}_D ₂ Direct Set Inputs
- Q₁, Q₂, \bar{Q}_1 , \bar{Q}_2 Outputs

TRUTH TABLE

Inputs					Outputs	
\bar{S}_D	\bar{C}_D	CP	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	L	H
H	H	↓	H	L	Toggle	
H	H	↓	L	H	Q ₀	\bar{Q}_0
H	H	↓	H	H	H	L
H	H	L	X	X	Q ₀	\bar{Q}_0

H = HIGH Voltage Level

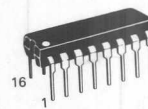
L = LOW Voltage Level

↓ = LOW-to-HIGH Clock Transition

X = Immaterial

Q₀(\bar{Q}_0) = Previous Q₀(\bar{Q}_0) before LOW-to-HIGH Transition of Clock

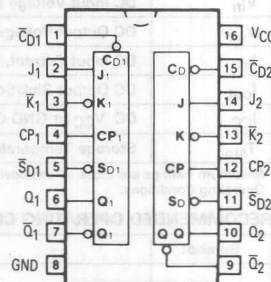
**DUAL JK̄ POSITIVE
EDGE-TRIGGERED
FLIP-FLOP**



**N SUFFIX
CASE 648-08
PLASTIC**

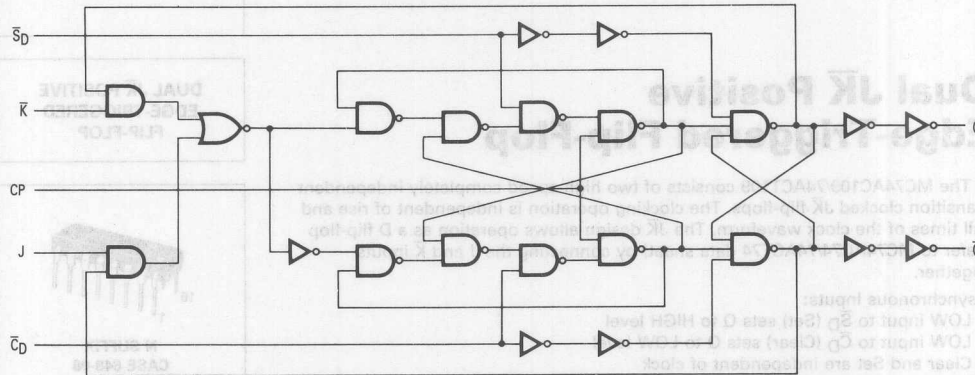


**D SUFFIX
CASE 751B-03
PLASTIC**



MC74AC109 • MC74ACT109

LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 \text{ V}$	150		ns/V
		$V_{CC} @ 4.5 \text{ V}$	40		
		$V_{CC} @ 5.5 \text{ V}$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 \text{ V}$	10		ns/V
		$V_{CC} @ 5.5 \text{ V}$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

FACT DATA

MC74AC109 • MC74ACT109

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

		Max	Min	Typ	Min	Max	
1-2	ns	120	120		2.5	2.5	Maximum Clock Frequency
2-3	ns	120	120		2.5	2.5	Propagation Delay C _P to Q _A or Q _B
3-2	ns	120	120		2.5	2.5	Propagation Delay Q _A to C _P or Q _B
3-3	ns	120	120		2.5	2.5	Propagation Delay Q _A to Q _B or Q _B to Q _A
3-4	ns	120	120		2.5	2.5	Propagation Delay Q _A to Q _C or Q _C to Q _A
3-5	ns	120	120		2.5	2.5	Propagation Delay Q _A to Q _D or Q _D to Q _A

V_{CC} = 5.0 V
V_{OH} = 3.85 V
V_{OL} = 0.1 V

FACT DATA

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	125 150			100 125		MHz	3-3
t _{PLH}	Propagation Delay C _{Pn} to Q _n or \overline{Q}_n	3.3 5.0	4.0 2.5		13.5 10.0	3.5 2.0	16.0 10.5	ns	3-6
t _{PHL}	Propagation Delay C _{Pn} to Q _n or \overline{Q}_n	3.3 5.0	3.0 2.0		14.0 10.0	3.0 1.5	14.5 10.5	ns	3-6
t _{PLH}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n	3.3 5.0	3.0 2.5		12.0 9.0	2.5 2.0	13.0 10.0	ns	3-6
t _{PHL}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n	3.3 5.0	3.0 2.0		12.0 9.5	3.0 2.0	13.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC109 • MC74ACT109

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW J _n or \bar{K}_n to CP _n	3.3 5.0		6.5 4.5	7.5 5.0	ns	3-9	
t _h	Hold Time, HIGH or LOW J _n or \bar{K}_n to CP _n	3.3 5.0		0 0.5	0 0.5	ns	3-9	
t _w	Pulse Width CP _n or \bar{C}_{Dn} or \bar{S}_{Dn}	3.3 5.0		4.0 3.5	4.5 3.5	ns	3-6	
t _{rec}	Recovery Time \bar{C}_{Dn} or \bar{S}_{Dn} to CP	3.3 5.0		0 0	0 0	ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	145			125		MHz	3-3
t _{PLH}	Propagation Delay C _{Pn} to Q _n or \bar{Q}_n	5.0	4.0		11.0	3.5	13.0	ns	3-6
t _{PHL}	Propagation Delay C _{Pn} to Q _n or \bar{Q}_n	5.0	3.0		10.0	2.5	11.5	ns	3-6
t _{PLH}	Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Q _n or \bar{Q}_n	5.0	2.5		9.5	2.0	10.5	ns	3-6
t _{PHL}	Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Q _n or \bar{Q}_n	5.0	2.5		10.0	2.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	VCC* (V)	74ACT		74ACT		Units	Fig No.
			TA = +25°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum				
ts	Set-up Time, HIGH or LOW Jn or Kn to CPn	5.0		2.0	2.5	ns	3-9	
th	Hold Time, HIGH or LOW Jn or Kn to CPn	5.0		2.0	2.0	ns	3-9	
tw	Pulse Width CPn or Cn or Sn	5.0		5.0	6.0	ns	3-6	
trec	Recovery Time Cn or Sn to CP	5.0		0	0	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	35	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

MC74AC132
MC74ACT132

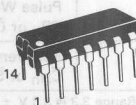
Quad 2-Input NAND Schmitt Trigger

The MC74AC/74ACT132 contains four 2-input NAND gates which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

- Schmitt Trigger Inputs
- Outputs Source/Sink 24 mA
- 'ACT132 Has TTL Compatible Inputs

**QUAD 2-INPUT
NAND
SCHMITT TRIGGER**

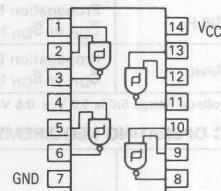


**N SUFFIX
CASE 646-06
PLASTIC**



**D SUFFIX
CASE 751A-02
PLASTIC**

PIN CONFIGURATION



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

FUNCTION TABLE

Inputs		Output
A	B	\bar{Y}
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level L = LOW Voltage Level

FACT DATA

MC74AC132 • MC74ACT132

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC132 • MC74ACT132

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC132 • MC74ACT132

INPUT CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	V _{CC} (V)	74AC	74ACT	Units	Test Conditions
V _{t+}	Maximum Positive Threshold	3.0 4.5 5.5	3.2 3.2 3.9	2.0	V	T _A = Worst Case
V _{t-}	Minimum Negative Threshold	3.0 4.5 5.5	0.5 0.9 1.1	0.8	V	T _A = Worst Case
V _{h(max)}	Maximum Hysteresis	3.0 4.5 5.5	1.2 1.4 1.6	1.2	V	T _A = Worst Case
V _{h(min)}	Minimum Hysteresis	3.0 4.5 5.5	0.3 0.4 0.5	0.4	V	T _A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5			1.0 1.0		ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5			1.0 1.0		ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	3.0		9.0	2.5	9.5	ns	3-6
t _{PHL}	Propagation Delay	5.0	3.0		9.0	2.5	9.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V



MOTOROLA

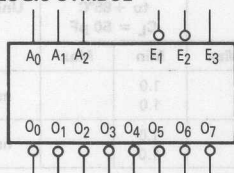
MC74AC138 MC74ACT138

1-of-8 Decoder/Demultiplexer

The MC74AC138/74ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three MC74AC138/74ACT138 devices or a 1-of-32 decoder using four MC74AC138/74ACT138 devices and one inverter.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- *ACT138 Has TTL Compatible Inputs

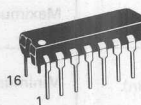
LOGIC SYMBOL



PIN NAMES

A₀-A₂ Address Inputs
 E₁-E₂ Enable Inputs
 E₃ Enable Input
 O₀-O₇ Outputs

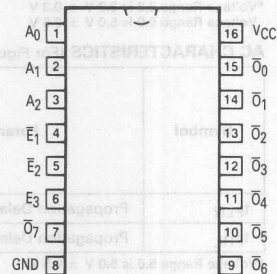
1-OF-8 DECODER/ DEMULPLEXER



N SUFFIX
 CASE 648-08
 PLASTIC



D SUFFIX
 CASE 751B-03
 PLASTIC



MC74AC138 • MC74ACT138

FUNCTIONAL DESCRIPTION

The MC74AC138/74ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0 , A_1 , A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs (\bar{O}_0 – \bar{O}_7). The MC74AC138/74ACT138 features three Enable inputs, two active-LOW (\bar{E}_1 , \bar{E}_2) and one active-HIGH (E_3). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enabled function allows easy parallel expansion of the

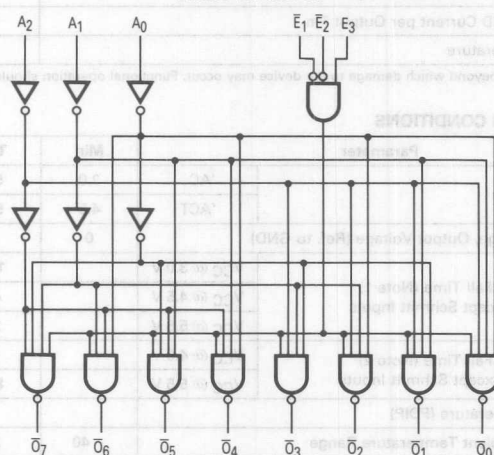
device to a 1-of-32 (5 lines to 32 lines) decoder with just four MC74AC138/74ACT138 devices and one inverter (See Figure a). The MC74AC138/74ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

TRUTH TABLE

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	L	L	L	H	H	H	H	H	H
L	L	H	L	L	L	L	H	L	H	H	H	H	H
L	L	H	L	L	L	L	H	H	L	H	H	H	H
L	L	H	L	L	L	L	H	H	H	L	H	H	H
L	L	H	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	H	H	H	H	H	L	H
L	L	H	L	L	L	L	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM

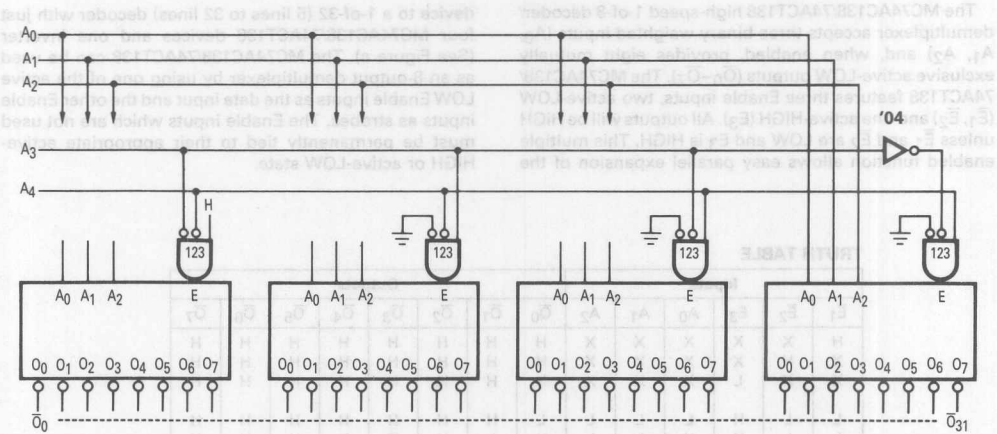


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

MC74AC138 • MC74ACT138

Figure a: Expansion to 1-of-32 Decoding



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	- 65 to + 150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 \text{ V}$	150		ns/V
		$V_{CC} @ 4.5 \text{ V}$	40		
		$V_{CC} @ 5.5 \text{ V}$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 \text{ V}$	10		ns/V
		$V_{CC} @ 5.5 \text{ V}$	8.0		
T_J	Junction Temperature (PDIP)			140	$^{\circ}\text{C}$
T_A	Operating Ambient Temperature Range	- 40	25	85	$^{\circ}\text{C}$
I_{OH}	Output Current — High			- 24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

FACT DATA

MC74AC138 • MC74ACT138

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC138 • MC74ACT138

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = – 50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC138 • MC74ACT138

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to O _n	3.3 5.0	1.5 1.5	8.5 6.5	13.0 9.5	1.5 1.5	15.0 10.5	ns	3-6
t _{PHL}	Propagation Delay A _n to O _n	3.3 5.0	1.5 1.5	8.0 6.0	12.5 9.0	1.5 1.5	14.0 10.5	ns	3-6
t _{PLH}	Propagation Delay E ₁ or E ₂ to O _n	3.3 5.0	1.5 1.5	11.0 8.0	15.0 11.0	1.5 1.5	16.0 12.0	ns	3-6
t _{PHL}	Propagation Delay E ₁ or E ₂ to O _n	3.3 5.0	1.5 1.5	9.5 7.0	13.5 9.5	1.5 1.5	15.0 10.5	ns	3-6
t _{PLH}	Propagation Delay E ₃ to O _n	3.3 5.0	1.5 1.5	11.0 8.0	15.5 11.0	1.5 1.5	16.5 12.5	ns	3-6
t _{PHL}	Propagation Delay E ₃ to O _n	3.3 5.0	1.5 1.5	8.5 6.0	13.0 8.0	1.5 1.0	14.0 9.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to O _n	5.0	1.5	7.0	10.5	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay A _n to O _n	5.0	1.5	6.5	10.5	1.5	11.5	ns	3-6
t _{PLH}	Propagation Delay E ₁ or E ₂ to O _n	5.0	2.5	8.0	11.5	2.0	12.5	ns	3-6
t _{PHL}	Propagation Delay E ₁ or E ₂ to O _n	5.0	2.0	7.5	11.5	2.0	12.5	ns	3-6
t _{PLH}	Propagation Delay E ₃ to O _n	5.0	2.5	8.0	12.0	2.0	13.0	ns	3-6
t _{PHL}	Propagation Delay E ₃ to O _n	5.0	2.0	6.5	10.5	1.5	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	60	pF	V _{CC} = 5.0 V



MOTOROLA

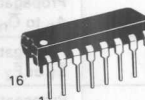
MC74AC139 MC74ACT139

Dual 1-of-4 Decoder/Demultiplexer

The MC74AC139/74ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the MC74AC139/74ACT139 can be used as a function generator providing all four minterms of two variables.

- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- 'ACT139 Has TTL Compatible Inputs

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

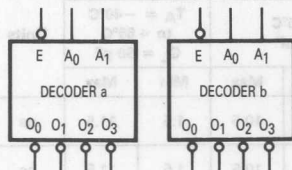


**N SUFFIX
CASE 648-08
PLASTIC**



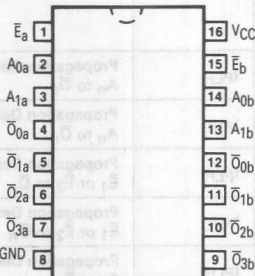
**D SUFFIX
CASE 751B-03
PLASTIC**

LOGIC SYMBOL



PIN NAMES

A₀, A₁ Address Inputs
E Enable Inputs
O₀–O₃ Outputs



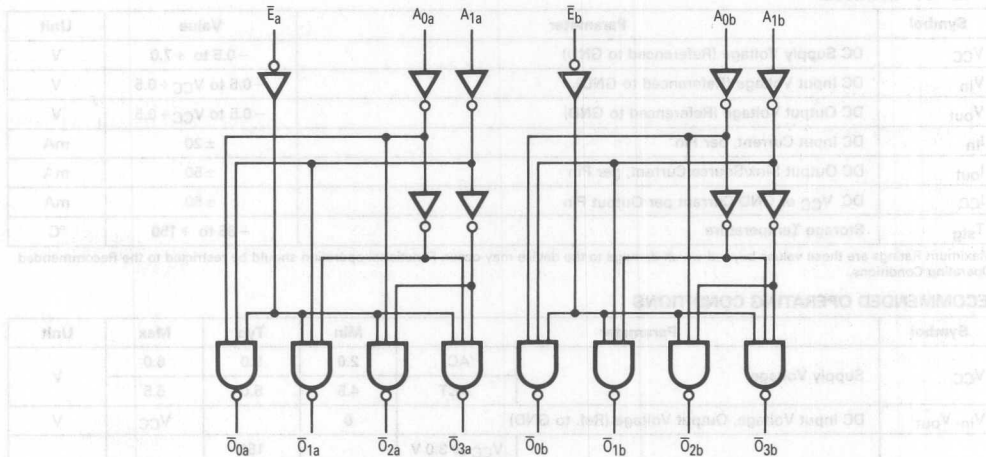
TRUTH TABLE

Inputs			Outputs			
\bar{E}	A ₀	A ₁	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MC74AC139 • MC74ACT139

LOGIC DIAGRAM

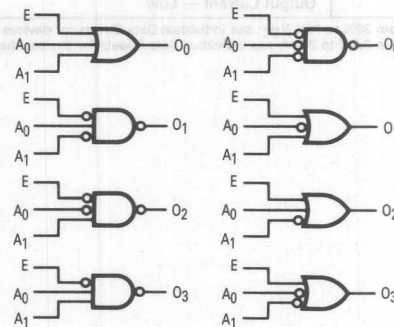


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC139/74ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0 – A_1) and provides four mutually exclusive active-LOW outputs (\bar{O}_0 – \bar{O}_3). Each decoder has an active-LOW enable (\bar{E}). When \bar{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the MC74AC139/74ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

Figure a: Gate Functions (each half)



MC74AC139 • MC74ACT139

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC138 • MC74ACT138

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC139 • MC74ACT139

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = –50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA –24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC139 • MC74ACT139

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to O _n	3.3 5.0	4.0 3.0	8.0 6.5	11.5 8.5	3.5 2.5	13 9.5	ns	3-6
t _{PHL}	Propagation Delay A _n to O _n	3.3 5.0	3.0 2.5	7.0 5.5	10 7.5	2.5 2.0	11 8.5	ns	3-6
t _{PLH}	Propagation Delay E _n to O _n	3.3 5.0	4.5 3.5	9.5 7.0	12 8.5	3.5 3.0	13 10	ns	3-6
t _{PHL}	Propagation Delay E _n to O _n	3.3 5.0	4.0 2.5	8.0 6.0	10 7.5	3.0 2.5	11 8.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to O _n	5.0	1.5	6.0	8.5	1.5	9.5	ns	3-6
t _{PHL}	Propagation Delay A _n to O _n	5.0	1.5	6.0	9.5	1.5	10.5	ns	3-6
t _{PLH}	Propagation Delay E _n to O _n	5.0	2.5	7.0	10.0	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay E _n to O _n	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V



MOTOROLA

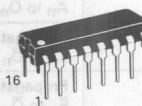
MC74AC151 MC74ACT151

1-of-8 Decoder/Demultiplexer

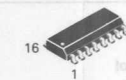
The MC74AC151/74ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The MC74AC151/74ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

- Outputs Source/Sink 24 mA
- 'ACT151 Has TTL Compatible Inputs

1-OF-8 DECODER/DEMULTIPLEXER



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**

LOGIC SYMBOL



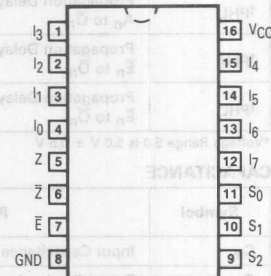
PIN NAMES

I ₀ -I ₇	Data Inputs
S ₀ -S ₂	Select Inputs
E	Enable Input
Z	Data Output
Z̄	Inverted Data Output

TRUTH TABLE

Inputs				Outputs	
Ē	S ₂	S ₁	S ₀	Z̄	Z
H	X	X	X	H	L
L	L	L	L	I ₀	I ₀
L	L	L	H	I ₁	I ₁
L	L	H	L	I ₂	I ₂
L	L	H	H	I ₃	I ₃
L	H	L	L	I ₄	I ₄
L	H	L	H	I ₅	I ₅
L	H	H	L	I ₆	I ₆
L	H	H	H	I ₇	I ₇

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



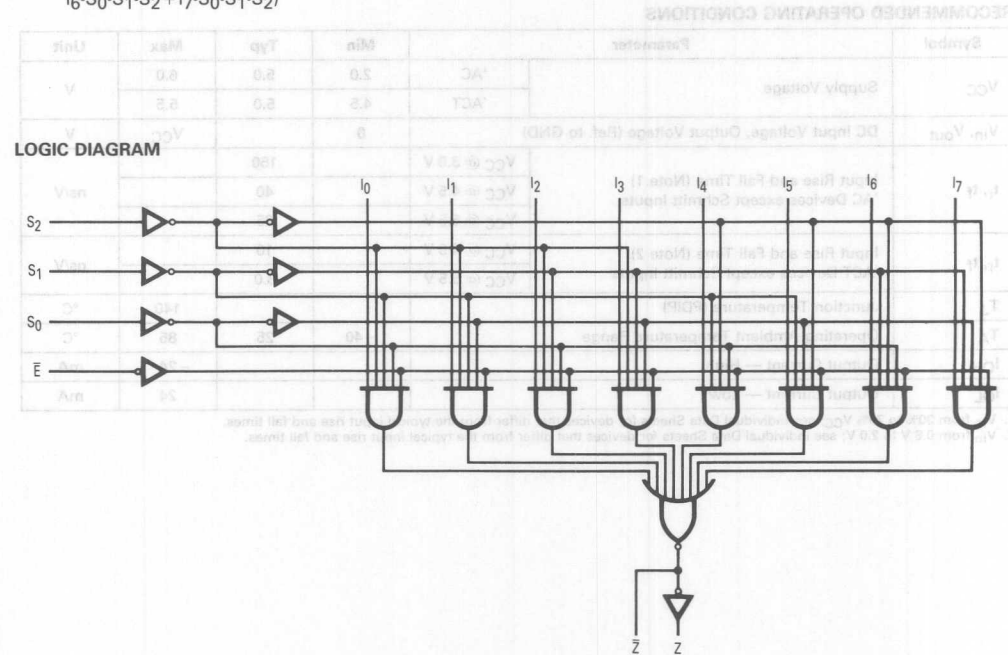
MC74AC151 • MC74ACT151

FUNCTIONAL DESCRIPTION

The MC74AC151/74ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both true and complementary outputs are provided. The Enable input (\bar{E}) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_4 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

The MC74AC151/74ACT151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the MC74AC151/74ACT151 can provide any logic function of four variables and its complement.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC151 • MC74ACT151

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC151 • MC74ACT151

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC151 • MC74ACT151

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = –50 μA	
		5.5	5.49	5.4	5.4			
	V	4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
	V	4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = –40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z or Z̄	3.3 5.0	3.0 2.5	11.5 8.5	18.0 13.0	3.0 2.0	20.0 15.0	ns	3-6
t _{PHL}	Propagation Delay S _n to Z or Z̄	3.3 5.0	2.5 2.0	12 8.5	18.0 13.0	2.5 1.5	20.0 15.0	ns	3-6
t _{PLH}	Propagation Delay E to Z or Z̄	3.3 5.0	2.5 2.0	8.0 6.0	13.0 10.0	2.0 1.5	14.0 11.0	ns	3-6
t _{PHL}	Propagation Delay E to Z or Z̄	3.3 5.0	1.5 1.5	8.5 6.5	13.0 10.0	1.5 1.5	14.0 11.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z or Z̄	3.3 5.0	2.5 1.5	9.5 7.0	14.0 10.5	2.0 1.5	15.5 11.0	ns	3-5
t _{PHL}	Propagation Delay I _n to Z or Z̄	3.3 5.0	2.5 1.5	9.5 7.0	15.0 11.0	2.0 1.5	16.0 12.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC151 • MC74ACT151



AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z	5.0	3.5		15.5	3.0	17.0	ns	3-6
t _{PHL}	Propagation Delay S _n to Z	5.0	3.5		15.5	3.0	16.5	ns	3-6
t _{PLH}	Propagation Delay S _n to Z̄	5.0	3.5		15	3.0	16.5	ns	3-6
t _{PHL}	Propagation Delay S _n to Z	5.0	4.0		16.5	3.5	18.5	ns	3-6
t _{PLH}	Propagation Delay E to Z	5.0	2.5		9.5	2.5	10.0	ns	3-6
t _{PHL}	Propagation Delay E to Z	5.0	2.5		9.0	2.5	10.0	ns	3-6
t _{PLH}	Propagation Delay E to Z̄	5.0	2.5		8.5	2.5	9.5	ns	3-6
t _{PHL}	Propagation Delay E to Z̄	5.0	3.0		10.0	2.5	10.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z	5.0	3.5		11.5	3.0	12.5	ns	3-6
t _{PHL}	Propagation Delay I _n to Z	5.0	3.5		12.0	3.0	13.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z̄	5.0	3.5		12.0	3.0	13.0	ns	3-6
t _{PHL}	Propagation Delay I _n to Z̄	5.0	4.0		12.5	3.0	14.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	70	pF	V _{CC} = 5.0 V

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	70	pF	V _{CC} = 5.0 V

H = HIGH Voltage Level
L = LOW Voltage Level
X = Unspecified

FACT DATA



MOTOROLA

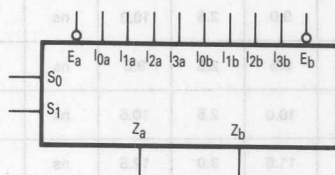
MC74AC153 MC74ACT153

Dual 4-Input Multiplexer

The MC74AC153/74ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the MC74AC153/74ACT153 can act as a function generator and generate any two functions of three variables.

- Outputs Source/Sink 24 mA
- ACT153 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

I0a-I3a Side A Data Inputs
I0b-I3b Side B Data Inputs
S0, S1 Common Select Inputs
Ea Side A Enable Input
Eb Side B Enable Input
Za Side A Output
Zb Side B Output

TRUTH TABLE

Select Inputs		Inputs (a or b)						Output
S0	S1	E	I0	I1	I2	I3	Z	
X	X	H	X	X	X	X	L	
L	L	L	L	X	X	X	L	
L	L	L	H	X	X	X	H	
H	L	L	X	L	X	X	L	
H	L	L	X	H	X	X	H	
L	H	L	X	X	L	X	L	
L	H	L	X	X	H	X	H	
H	H	L	X	X	X	L	L	
H	H	L	X	X	X	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

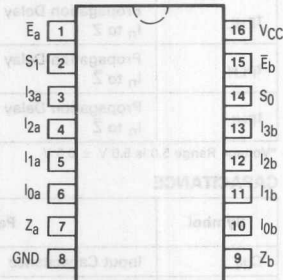
DUAL 4-INPUT MULTIPLEXER



N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC



MC74AC153 • MC74ACT153

FUNCTIONAL DESCRIPTION

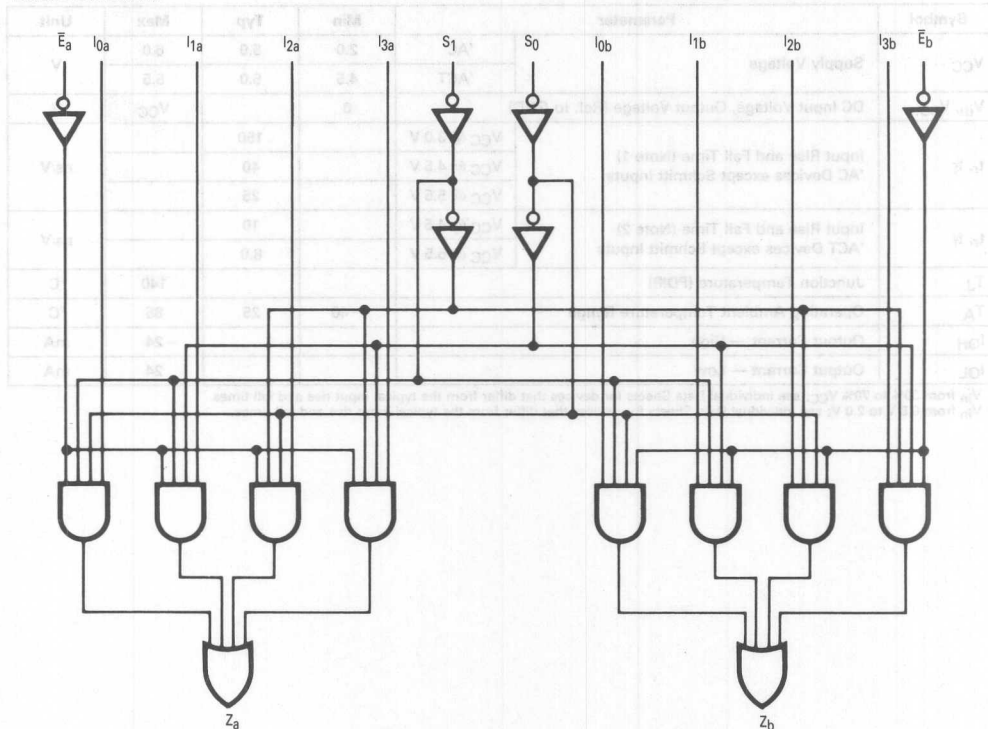
The MC74AC153/74ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active-LOW Enables (\bar{E}_a , \bar{E}_b) which can be used to strobe the outputs independently. When the Enables (\bar{E}_a , \bar{E}_b) are HIGH, the corresponding outputs (Z_a , Z_b) are forced LOW. The MC74AC153/74ACT153 is the logic

implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC153 • MC74ACT153

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC153 • MC74ACT153

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC153 • MC74ACT153

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC153 • MC74ACT153



AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _N to Z _N	3.3 5.0	2.5 2.0	9.5 6.5	15.0 11.0	2.5 2.0	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay S _N to Z _N	3.3 5.0	3.0 2.5	8.5 6.5	14.5 11.0	2.5 2.0	16.5 12.0	ns	3-6
t _{PLH}	Propagation Delay E _N to Z _N	3.3 5.0	2.5 1.5	8.0 5.5	13.5 9.5	2.0 1.5	16.0 11.0	ns	3-6
t _{PHL}	Propagation Delay E _N to Z _N	3.3 5.0	2.5 2.0	7.0 5.0	11.0 8.0	2.0 1.5	12.5 9.0	ns	3-6
t _{PLH}	Propagation Delay I _N to Z _N	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	2.0 1.5	14.5 10.5	ns	3-5
t _{PHL}	Propagation Delay I _N to Z _N	3.3 5.0	1.5 1.5	7.0 5.0	11.5 8.5	1.5 1.5	13.0 10.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	5.0	3.0	7.0	11.5	2.0	13.5	ns	3-6
t _{PHL}	Propagation Delay S _n to Z _n	5.0	3.0	7.0	11.5	2.5	13.5	ns	3-6
t _{PLH}	Propagation Delay E _n to Z _n	5.0	2.0	6.5	10.5	2.0	12.5	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	5.0	3.0	6.0	9.5	2.5	11.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	2.5	5.5	9.5	2.0	11.0	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	5.0	2.0	5.5	9.5	2.0	11.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

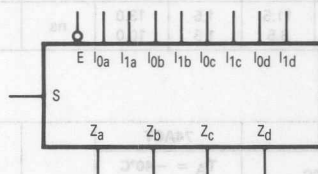
CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	65	pF	V _{CC} = 5.0 V

**MOTOROLA****MC74AC157
MC74ACT157****Quad 2-Input Multiplexer**

The MC74AC157/74ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The MC74AC157/74ACT157 can also be used as a function generator.

- Outputs Source/Sink 24 mA
- 'ACT157 Has TTL Compatible Inputs

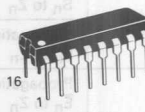
LOGIC SYMBOL**PIN NAMES**

I_{0a}-I_{0d} Source 0 Data Inputs
 I_{1a}-I_{1d} Source 1 Data Inputs
 E Enable Input
 S Select Input
 Z_a-Z_d Outputs

TRUTH TABLE

Inputs	Outputs			
\bar{E}	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

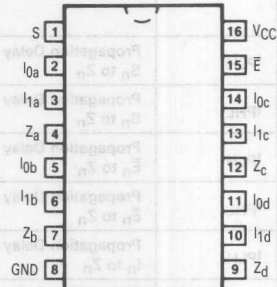
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

**QUAD 2-INPUT
MULTIPLEXER**

N SUFFIX
 CASE 648-08
 PLASTIC



D SUFFIX
 CASE 751B-03
 PLASTIC



MC74AC157 • MC74ACT157

FUNCTIONAL DESCRIPTION

The MC74AC157/74ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (E) is active-LOW. When E is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The MC74AC157/74ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

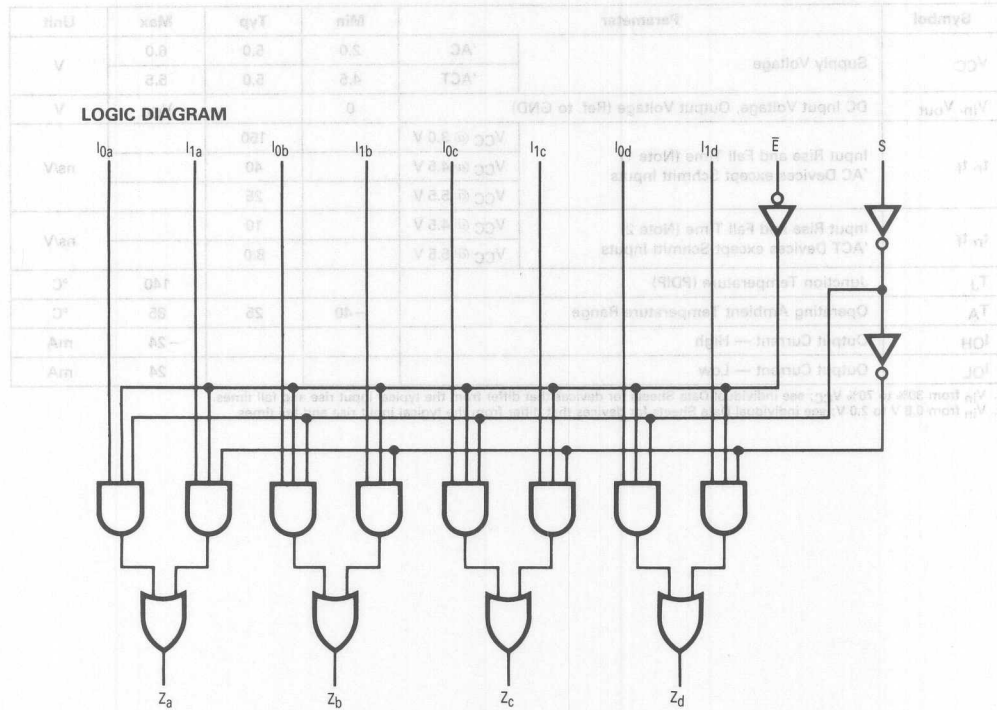
$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the MC74AC157/74ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC157/74ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC157 • MC74ACT157

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC157 • MC74ACT157

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC157 • MC74ACT157

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}	Output Current	5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC157 • MC74ACT157



AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.5 1.5	13.0 10.0	ns	3-6
t _{PHL}	Propagation Delay S to Z _n	3.3 5.0	1.5 1.5	6.5 5.0	11.0 8.5	1.5 1.0	12.0 9.5	ns	3-6
t _{PLH}	Propagation Delay E to Z _n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.5 1.5	13.0 10.0	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	3.3 5.0	1.5 1.5	6.5 5.5	11.0 9.0	1.5 1.0	12 9.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5	5.0 4.0	8.5 6.5	1.0 1.0	9.0 7.0	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5	5.0 4.0	8.0 6.5	1.0 1.0	9.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	5.0	2.0		9.0	1.5	10.0	ns	3-6
t _{PHL}	Propagation Delay S to Z _n	5.0	2.0		9.5	2.0	10.5	ns	3-6
t _{PLH}	Propagation Delay E _n to Z _n	5.0	1.5		10	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	5.0	1.5		8.5	1.0	9.0	n	3-6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	1.5		7.0	1.0	8.5	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	5.0	1.5		7.5	1.0	8.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V



MOTOROLA

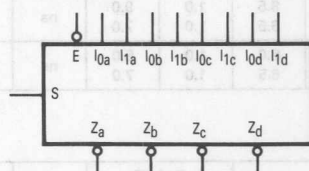
MC74AC158 MC74ACT158

Quad 2-Input Multiplexer

The MC74AC158/74ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The MC74AC158/74ACT158 can also be used as a function generator.

- Outputs Source/Sink 24 mA
- 'ACT158 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

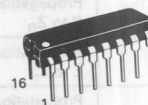
I0a-I0d	Source 0 Data Inputs
I1a-I1d	Source 1 Data Inputs
E	Enable Input
S	Select Input
Za-Zd	Inverted Outputs

TRUTH TABLE

Inputs				Outputs
E	S	I0	I1	Z
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

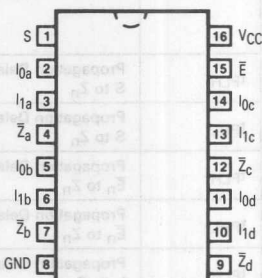
QUAD 2-INPUT MULTIPLEXER



N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

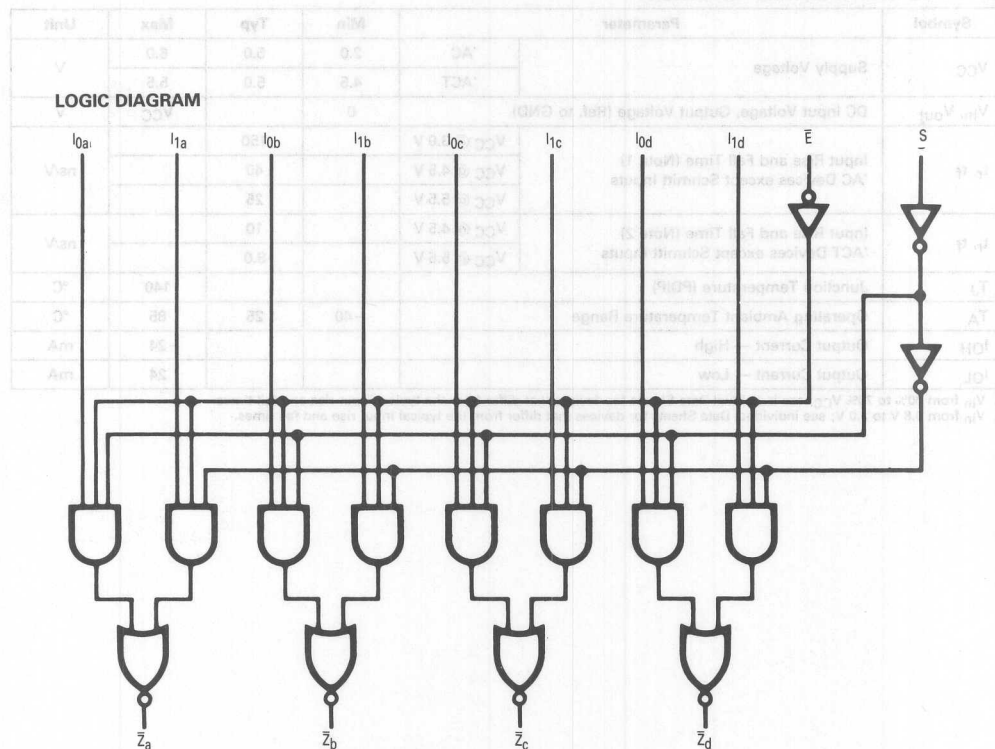


MC74AC158 • MC74ACT158

FUNCTIONAL DESCRIPTION

The MC74AC158/74ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (\bar{Z}) are forced HIGH regardless of all other inputs. The MC74AC158/74ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the MC74AC158/74ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC158/74ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC158 • MC74ACT158

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC158 • MC74ACT158

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
	V	3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
	V	3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC158 • MC74ACT158

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC158 • MC74ACT158



AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	3.3 5.0	1.5 1.5		11.5 9.0	1.5 1.0	12.5 9.5	ns	3-6
t _{PHL}	Propagation Delay S to Z _n	3.3 5.0	1.5 1.5		11.5 9.0	1.5 1.5	12.5 10.0	ns	3-6
t _{PLH}	Propagation Delay E to Z _n	3.3 5.0	1.5 1.5		12.0 9.5	1.5 1.5	13.0 10.5	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	3.3 5.0	1.5 1.5		11.0 8.5	1.5 1.0	12.0 9.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5		9.0 7.0	1.5 1.0	10.0 7.5	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5		8.0 6.5	1.0 1.0	8.5 6.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	5.0	2.5	6.0	9.5	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay S to Z _n	5.0	1.5	5.5	9.0	1.5	10.0	ns	3-6
t _{PLH}	Propagation Delay E _n to Z _n	5.0	1.5	5.5	9.5	1.5	10.5	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	5.0	1.5	5.5	9.5	1.5	10.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	1.5	4.5	8.0	1.0	8.5	ns	3-6
t _{PHL}	Propagation Delay I _n to Z _n	5.0	1.5	4.0	6.5	1.0	7.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



MOTOROLA

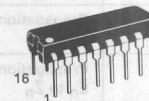
**MC74AC160
MC74ACT160
MC74AC162
MC74ACT162**

Synchronous Presettable BCD Decade Counter

The MC74AC160/74ACT160 and MC74AC162/74ACT162 are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC160/74ACT160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC162/74ACT162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz
- Outputs Source/Sink 24 mA
- 'ACT160 and 'ACT162 Have TTL Compatible Inputs

**SYNCHRONOUS
PRESETTABLE
BCD DECADE COUNTER**

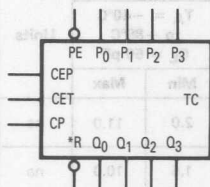


**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**

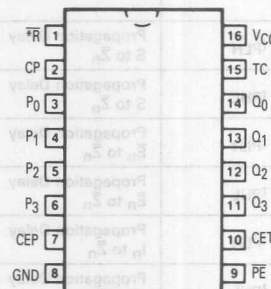
LOGIC SYMBOL



• \overline{MR} for '160
• SR for '162

PIN NAMES

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
\overline{MR} ('160)	Asynchronous Master Reset Input
SR ('162)	Synchronous Reset Input
P0-P3	Parallel Data Inputs
PE	Parallel Enable Input
Q0-Q3	Flip-Flop Outputs
TC	Terminal Count Output



FUNCTIONAL DESCRIPTION

The MC74AC160/74ACT160 and MC74AC162/74ACT162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('160), synchronous reset ('162), parallel load, count-up and hold. Five control inputs — Master Reset (\overline{MR} , '160), Synchronous Reset (\overline{SR} , '162), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on \overline{MR} overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \overline{SR} overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and \overline{MR} ('160) or \overline{SR} ('162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC160/74ACT160 and MC74AC162/74ACT162 use D-type edge-triggered flip-flops and changing the \overline{SR} , PE, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the MC74AC160/74ACT160 and MC74AC162/74ACT162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \cdot CET \cdot PE$

$$TC = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot CET$$

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (\uparrow)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

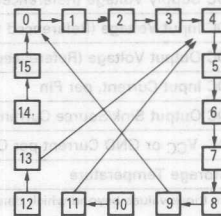
*For '162 only

H = HIGH Voltage Level

L = LOW Voltage Level

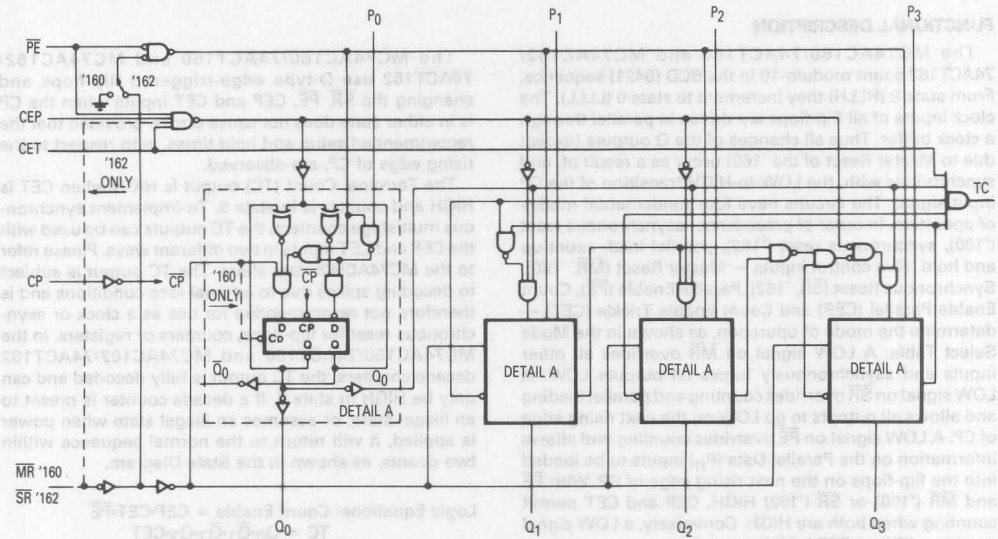
X = Immaterial

STATE DIAGRAM



MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	- 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High ¹			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

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FACT DATA

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC160/162			74AC160/162		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
fmax	Maximum Count Frequency	3.3 5.0		87 118				MHz	3-3
tPLH	Propagation Delay CP to Qn (PE Input HIGH)	3.3 5.0		7.5 5.5				ns	3-6
tPHL	Propagation Delay CP to Qn (PE Input HIGH)	3.3 5.0		8.5 6.0				ns	3-6
tPLH	Propagation Delay CP to Qn (PE Input LOW)	3.3 5.0		9.5 7.0				ns	3-6
tPHL	Propagation Delay CP to Qn (PE Input LOW)	3.3 5.0		9.5 7.0				ns	3-6
tPLH	Propagation Delay CP to TC	3.3 5.0		9.5 7.0				ns	3-6
tPHL	Propagation Delay CP to TC	3.3 5.0		11 8.0				ns	3-6
tPLH	Propagation Delay CET to TC	3.3 5.0		7.5 5.5				ns	3-6
tPHL	Propagation Delay CET to TC	3.3 5.0		8.5 6.0				ns	3-6
tPHL	Propagation Delay MR to Qn (*AC160)	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC160/162		74AC160/162	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0	5.5 4.0			ns	3-9
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0	-7.0 -5.0			ns	3-9
t _s	Setup Time, HIGH or LOW PE or SR to CP	3.3 3.3	5.5 4.0			ns	3-9
t _h	Hold Time, HIGH or LOW PE or SR to CP	3.3 5.0	-7.5 -5.5			ns	3-9
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5			ns	3-9
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	-4.5 -3.0			ns	3-9
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t _w	MR Pulse Width, LOW (AC160)	3.3 5.0	4.5 3.0			ns	3-6
t _{rec}	Recovery Time MR to CP (AC160)	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

MC74ACT160

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT160			74ACT160		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	120			100		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (P _E Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (P _E Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PLH}	Propagation Delay CP to Q _n (P _E Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (P _E Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	2.0	8.0	12.0	2.0	14.0	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	2.0	8.0	12.0	2.0	14.0	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	2.0	6.0	8.0	2.0	9.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	2.0	7.0	9.5	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.5	6.0	9.5	1.5	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

MC74ACT162

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT162			74ACT162		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	120			100		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (P _E Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (P _E Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PLH}	Propagation Delay CP to Q _n (P _E Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (P _E Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	2.0	8.0	12.0	2.0	14.0	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	2.0	8.0	12.0	2.0	14.0	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	2.0	6.0	8.0	2.0	9.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	8.0	2.0	9.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

MC74ACT160
AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT160		74ACT160		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	4.0	6.5	8.0	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	-4.0	-0.5	0	ns	3-9	
t _s	Setup Time, HIGH or LOW PE or MR to CP	5.0	4.0	8.5	10.5	ns	3-9	
t _h	Hold Time, HIGH or LOW PE or MR to CP	5.0	-4.0	0	0	ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	3.0	6.0	7.0	ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0	0	ns	3-9	
t _w	Clock Pulse Width (Load) HIGH or LOW	5.0	3.0	4.0	4.0	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	3.0	4.0	4.0	ns	3-6	
t _w	MR Pulse Width, LOW (ACT160)	5.0	2.0	4.0	6.0	ns	3-6	
t _{rec}	Recovery Time MR to CP (ACT160)	5.0	-1.0	0	0	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	Value Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pf	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	35	pf	V _{CC} = 5.0 V

MC74AC160 • MC74ACT160 • MC74AC162 • MC74ACT162

MC74ACT162
AC OPERATING REQUIREMENTS

Symbol	Parameter	VCC* (V)	74ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Pn to CP	5.0	4.0	7.0	10.0	ns	3-9	
th	Hold Time, HIGH or LOW Pn to CP	5.0	-3.0	-1.0	0	ns	3-9	
ts	Setup Time, HIGH or LOW PE to CP	5.0	4.0	7.0	10.0	ns	3-9	
th	Hold Time, HIGH or LOW PE to CP	5.0	-3.0	-1.0	0	ns	3-9	
ts	Setup Time, HIGH or LOW SR to CP	5.0	5.0	10	11.5	ns	3-9	
th	Hold Time, HIGH or LOW SR to CP	5.0	-5.0	0	0	ns	3-9	
ts	Setup Time, HIGH or LOW CET to CP	5.0	3.0	6.0	7.0	ns	3-9	
th	Hold Time, HIGH or LOW CET to CP	5.0	-3.0	0	0	ns	3-9	
tw	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	4.5	5.0	ns	3-6	
tw	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	4.0	4.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



MOTOROLA

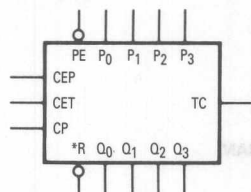
**MC74AC161
MC74ACT161
MC74AC163
MC74ACT163**

Synchronous Presettable Binary Counter

The MC74AC161/74ACT161 and MC74AC163/74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC161/74ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC163/74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- 'ACT161 and 'ACT163 Have TTL Compatible Inputs

LOGIC SYMBOL

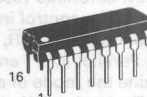


*MR for '161
*SR for '163

PIN NAMES

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
MR ('161)	Asynchronous Master Reset Input
SR ('163)	Synchronous Reset Input
P0-P3	Parallel Data Inputs
PE	Parallel Enable Input
Q0-Q3	Flip-Flop Outputs
TC	Terminal Count Output

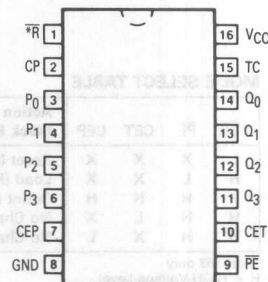
SYNCHRONOUS PRESETTABLE BINARY COUNTER



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**





FUNCTIONAL DESCRIPTION

The MC74AC161/74ACT161 and MC74AC163/74ACT163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs — Master Reset (MR, '161), Synchronous Reset (SR, '163), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded

into the flip-flops on the next rising edge of CP. With PE and MR ('161) or SR ('163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC161/74ACT161 and MC74AC163/74ACT163 use D-type edge-triggered flip-flops and changing the SR, PE, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = $CEP \cdot CET \cdot PE$

$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge ()
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

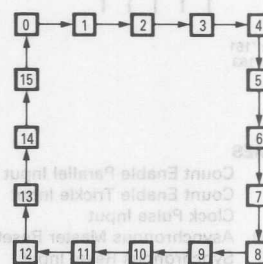
*For '163 only

H = HIGH Voltage Level

L = LOW Voltage Level

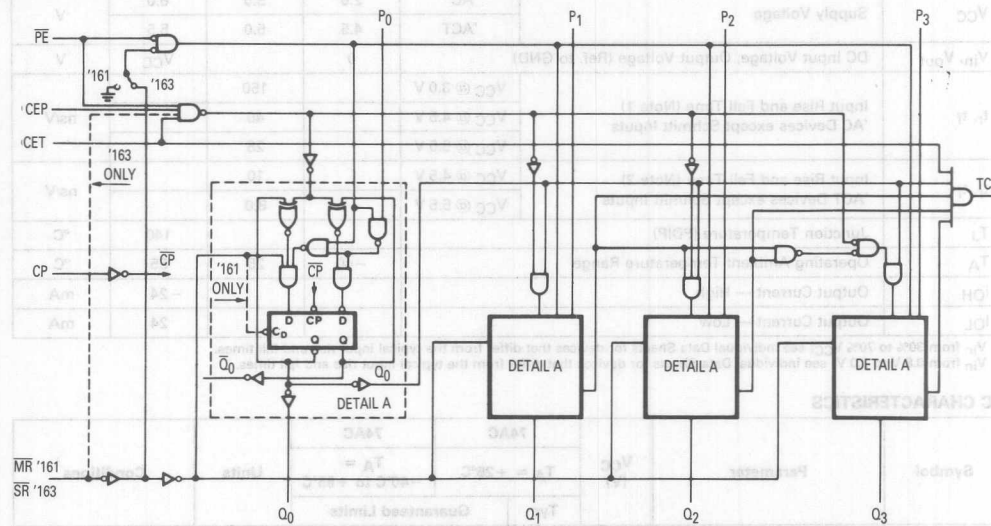
X = Immaterial

STATE DIAGRAM



MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

BLOCK DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Symbol	Parameter	Value	Unit
I_{in}	Maximum Input Leakage Current	10	nA
I_{OH}	Maximum Output Current	50	mA
I_{OL}	Maximum Output Current	50	mA
I_{CC}	Maximum Quiescent Current	10	mA

FACT DATA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
V _{OL}	Maximum Low Level Output Voltage	3.0		2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA
		4.5		3.86	3.76			
		5.5		4.86	4.76			
I _{IN}	Maximum Input Leakage Current	5.5	±0.1	±1.0		μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5		75		mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5		-75		mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	8.0	80		μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC161			74AC161		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167		60 95		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (P _E Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12.0 9.0	1.5 1.0	13.5 9.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (P _E Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.0 6.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14.0 11.0	2.5 2.0	15.5 11.5	ns	3-6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3-6
t _{PLH}	Propagation Delay MR to Q _n	3.3 5.0	2.0 1.5	6.0 5.5	12.0 9.5	1.5 1.5	13.5 10.0	ns	3-6
t _{PHL}	Propagation Delay MR to TC	3.3 5.0	3.5 2.5	10.0 8.5	15.0 13.0	3.0 2.5	17.5 13.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC161		74AC161	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0	6.0 3.5	13.5 8.5	16.0 10.5	ns	3-9
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0	-7.0 -4.0	-1.0 0	-0.5 0	ns	3-9
t _s	Setup Time, HIGH or LOW PE to CP	3.3 5.0	6.5 4.0	11.5 7.5	14.0 8.5	ns	3-9
t _h	Hold Time, HIGH or LOW PE to CP	3.3 5.0	-6.0 -3.5	0 0.5	0 1.0	ns	3-9
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.0 2.0	6.0 4.5	7.0 5.0	ns	3-9
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	-3.5 -2.0	0 0	0 0.5	ns	3-9
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	2.0 2.0	3.5 2.5	4.0 3.0	ns	3-6
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	2.0 2.0	4.0 3.0	4.5 3.5	ns	3-6
t _w	MR Pulse Width, LOW	3.3 5.0	3.0 2.5	5.5 4.5	7.5 6.0	ns	3-6
t _{rec}	Recovery Time MR to CP	3.3 5.0	-2.0 -1.0	-0.5 0	0 0.5	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT161			74ACT161		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	115	125		100		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.5	8.0	10.0	1.5	13.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.5	8.0	10.0	1.5	12.5	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	2.0	11.0	13.5	1.5	16.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	1.5	11.0	13.0	1.5	15.5	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	1.5	7.5	9.0	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	1.5	8.0	10.0	1.5	13.0	ns	3-6
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.5	8.0	9.5	1.5	12.0	ns	3-6
t _{PHL}	Propagation Delay MR to TC	5.0	2.5	10	11.5	2.0	14.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT161		74ACT161		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	7.0	8.5	11.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	−3.0	−1.0	0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW P _E to CP	5.0	6.0	7.5	10.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _E to CP	5.0	−3.5	0	0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW C _{EP} or C _{ET} to CP	5.0	4.0	5.5	9.5	ns	3-9	
t _h	Hold Time, HIGH or LOW C _{EP} or C _{ET} to CP	5.0	−2.0	0	0.5	ns	3-9	
t _w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	4.5	6.5	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	4.5	6.5	ns	3-6	
t _w	MR Pulse Width, LOW	5.0	3.0	4.5	6.5	ns	3-6	
t _{rec}	Recovery Time MR to CP	5.0	0	0	0.5	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC163			74AC163		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
fmax	Maximum Count Frequency	3.3 5.0	70 110	95 140		60 95		MHz	3-3
tPLH	Propagation Delay CP to Qn (PE Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.5 1.0	13.5 9.5	ns	3-6
tPHL	Propagation Delay CP to Qn (PE Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3-6
tPLH	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3-6
tPHL	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	2.5 2.0	15.5 11.5	ns	3-6
tPLH	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3-6
tPHL	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC163		74AC163		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0	5.5 4.0	13.5 8.5	16.0 10.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0	-7.0 -5.0	-1.0 0	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW SR to CP	3.3 5.0	5.5 4.0	14 9.5	16.5 11.0	ns	3-9	
t _h	Hold Time, HIGH or LOW SR to CP	3.3 5.0	-7.5 -5.5	-1.0 -0.5	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW PE to CP	3.3 5.0	5.5 4.0	11.5 7.5	14.0 8.5	ns	3-9	
t _h	Hold Time, HIGH or LOW PE to CP	3.3 5.0	-7.5 -5.0	-1.0 -0.5	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	7.0 5.0	ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	-4.5 -3.0	0 0	0 0.5	ns	3-9	
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	4.0 3.0	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns	3-6	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT163			74ACT163		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	120	140		105		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (P _E Input HIGH or LOW)	5.0	1.5	5.5	10.0	1.5	11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (P _E Input HIGH or LOW)	5.0	1.5	6.0	11.0	1.5	12.0	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5	2.0	13.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5	2.0	15.0	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0	1.5	10.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

SymbolParameter		V _{CC} * (V)	74ACT163		74ACT163	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	4.0	10.0	12.0	ns	3-9
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	-5.0	0.5	0.5	ns	3-9
t _s	Setup Time, HIGH or LOW SR to CP	5.0	4.0	10.0	11.5	ns	3-9
t _h	Hold Time, HIGH or LOW SR to CP	5.0	-5.5	-0.5	-0.5	ns	3-9
t _s	Setup Time, HIGH or LOW PE to CP	5.0	4.0	8.5	10.5	ns	3-9
t _h	Hold Time, HIGH or LOW PE to CP	5.0	-5.5	-0.5	0	ns	3-9
t _s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3-9
t _h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0	0.5	ns	3-9
t _w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Type	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

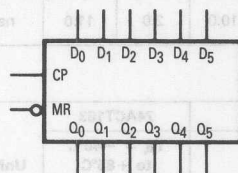
**MC74AC174
MC74ACT174**

Hex D Flip-Flop with Master Reset

The MC74AC174/74ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- Outputs Source/Sink 24 mA
- 'ACT174 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

D₀-D₅ Data Inputs
CP Clock Pulse Input
MR Master Reset Input
Q₀-Q₅ Outputs

TRUTH TABLE

Inputs			Output
MR	CP	D	Q
L	X	X	L
H	↓	H	H
H	↓	L	L
H	L	X	Q

H = HIGH Voltage Level
L = LOW Voltage Level

X = Immaterial

↓ = LOW-to-HIGH Transition of Clock

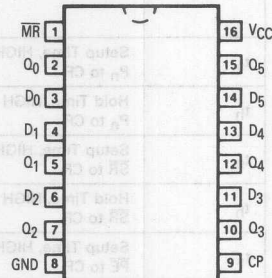
HEX D FLIP-FLOP WITH MASTER RESET



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**



FACT DATA

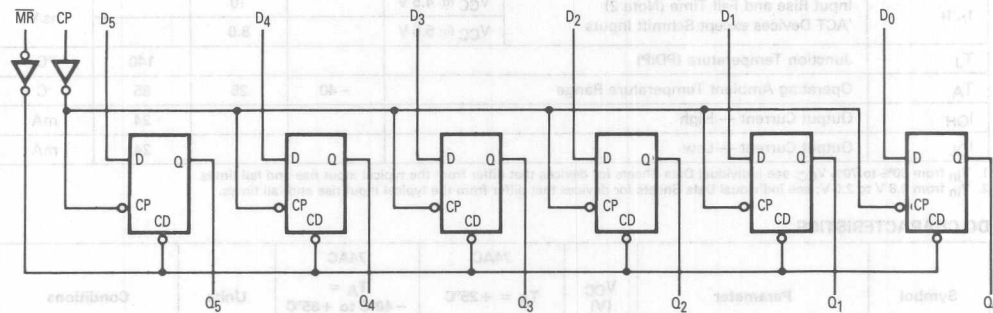
MC74AC174 • MC74ACT174

FUNCTIONAL DESCRIPTION

The MC74AC174/74ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (\overline{MR}) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the

Master Reset (\overline{MR}) will force all outputs LOW independent of Clock or Data inputs. The MC74AC174/74ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC, V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC, V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

FACT DATA

MC74AC174 • MC74ACT174

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V		150	
		V _{CC} @ 4.5 V		40	
		V _{CC} @ 5.5 V		25	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V		10	
		V _{CC} @ 5.5 V		8.0	
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	– 40	25	85	°C
I _{OH}	Output Current — High			– 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions				
			T _A = +25°C		T _A = –40°C to +85°C							
			Typ	Guaranteed Limits								
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V					
		4.5	2.25	3.15	3.15							
		5.5	2.75	3.85	3.85							
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V					
		4.5	2.25	1.35	1.35							
		5.5	2.75	1.65	1.65							
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA					
		4.5	4.49	4.4	4.4							
		5.5	5.49	5.4	5.4							
			3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA				
			4.5		3.86	3.76						
			5.5		4.86	4.76						
			V _{OL}	Maximum Low Level Output Voltage	3.0	0.002			0.1	0.1	V	I _{OUT} = 50 μA
					4.5	0.001			0.1	0.1		
					5.5	0.001			0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA					
		4.5		0.36	0.44							
		5.5		0.36	0.44							
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND					
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max					
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min					
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND					

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC174 • MC74ACT174

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
V _{OL}	Maximum Low Level Output Voltage	4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA I _{OUT} = 50 μA	
		5.5		4.86	4.76			
		4.5	0.001	0.1	0.1	V		
		5.5	0.001	0.1	0.1			
I _{IN}	Maximum Input Leakage Current	4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125		70 100		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _N	3.3 5.0	2.0 1.5	9.0 6.0	11.5 8.5	1.5 1.0	12.5 9.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _N	3.3 5.0	2.0 1.5	8.5 6.0	11.0 8.0	1.5 1.0	12.0 9.0	ns	3-6
t _{PHL}	Propagation Delay MR to Q _N	3.3 5.0	2.5 1.5	9.0 7.0	11.5 9.0	2.0 1.5	12.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3	2.5	6.5	7.0	ns	3-9	
		5.0	2.0	5.0	5.5			
t _h	Hold Time, HIGH or LOW D _n to CP	3.3	1.0	3.0	3.0	ns	3-9	
		5.0	0.5	3.0	3.0			
t _w	MR Pulse Width, LOW	3.3	1.0	5.5	7.0	ns	3-6	
		5.0	1.0	5.0	5.0			
t _w	CP Pulse Width	3.3	1.0	5.5	7.0	ns	3-6	
		5.0	1.0	5.0	5.0			
t _{rec}	Recovery Time MR to CP	3.3	0	2.5	2.5	ns	3-6	
		5.0	0	2.0	2.0			

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC174 • MC74ACT174

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	165			140		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n	5.0	1.5		10.5	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n	5.0	1.5		10.5	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.5		9.5	1.5	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0		1.5	1.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0		2.0	2.0	ns	3-9	
t _w	MR Pulse Width, LOW	5.0		3.0	3.5	ns	3-6	
t _w	CP Pulse Width HIGH or LOW	5.0		3.0	3.5	ns	3-6	
t _{rec}	Recovery Time MR to CP	5.0		0.5	0.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

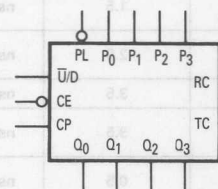
CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	85	pF	V _{CC} = 5.0 V

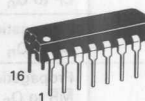
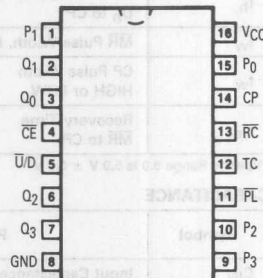
**MOTOROLA****MC74AC190****Up/Down Counter
with Preset and Ripple Clock**

The MC74AC190 is a reversible BCD (8421) decade counter which features synchronous counting and asynchronous presetting. The preset feature allows the MC74AC190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- High-Speed — 120 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Cascadable
- Outputs Source/Sink 24 mA

LOGIC SYMBOL**PIN NAMES**

\overline{CE}	Count Enable Input
CP	Clock Pulse Input
P_0 – P_3	Parallel Data Inputs
PL	Asynchronous Parallel Load Input
U/D	Up/Down Count Control Input
Q_0 – Q_3	Flip-Flop Outputs
RC	Ripple Clock Output
TC	Terminal Count Output

**UP/DOWN COUNTER
WITH PRESET
AND RIPPLE CLOCK****N SUFFIX
CASE 648-08
PLASTIC****D SUFFIX
CASE 751B-03
PLASTIC**

MC74AC190

FUNCTIONAL DESCRIPTION

The MC74AC190 is a synchronous up/down BCD decade counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Load inputs (P_0 – P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U/D}$ input signal, as indicated in the Mode Select Table. \overline{CE} and $\overline{U/D}$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 9 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U/D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the \overline{RC} outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the \overline{RC} output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The \overline{CE} input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

MODE SELECT TABLE

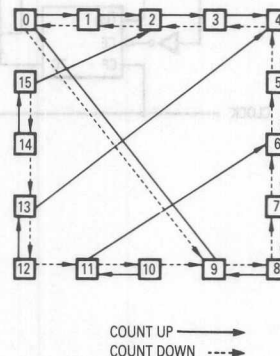
Inputs				Mode
\overline{PL}	\overline{CE}	$\overline{U/D}$	CP	
H	L	L	\downarrow	Count Up
H	L	H	\downarrow	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

Inputs				Outputs
\overline{PL}	\overline{CE}	TC*	CP	\overline{RC}
H	L	H	\downarrow	\downarrow
H	H	X	X	H
H	X	L	X	H
L	X	X	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 \downarrow = LOW-to-HIGH Transition

STATE DIAGRAM



FACT DATA

MC74AC190

Figure a: N-Stage Counter Using Ripple Clock

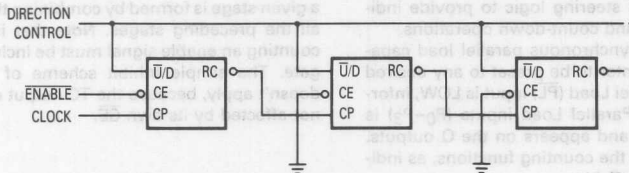


Figure b: Synchronous N-Stage Counter Using Ripple Carry/Borrow

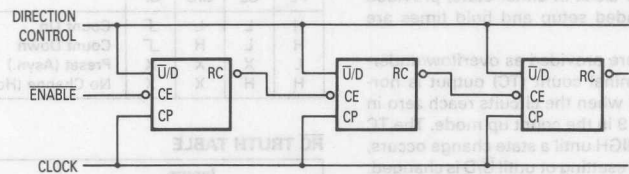
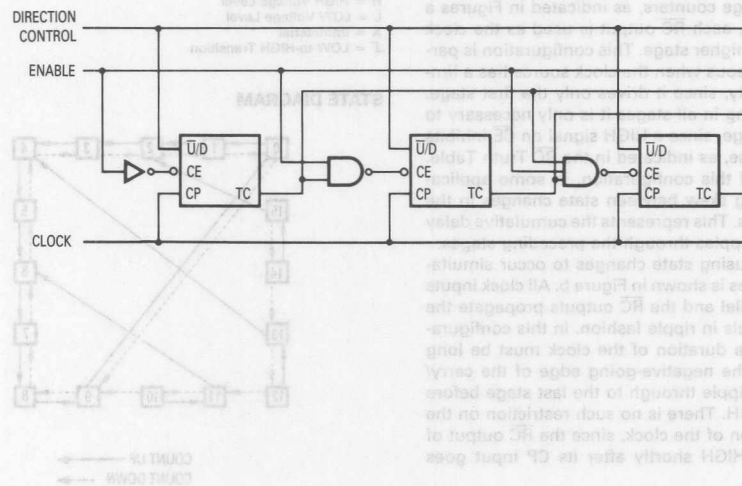
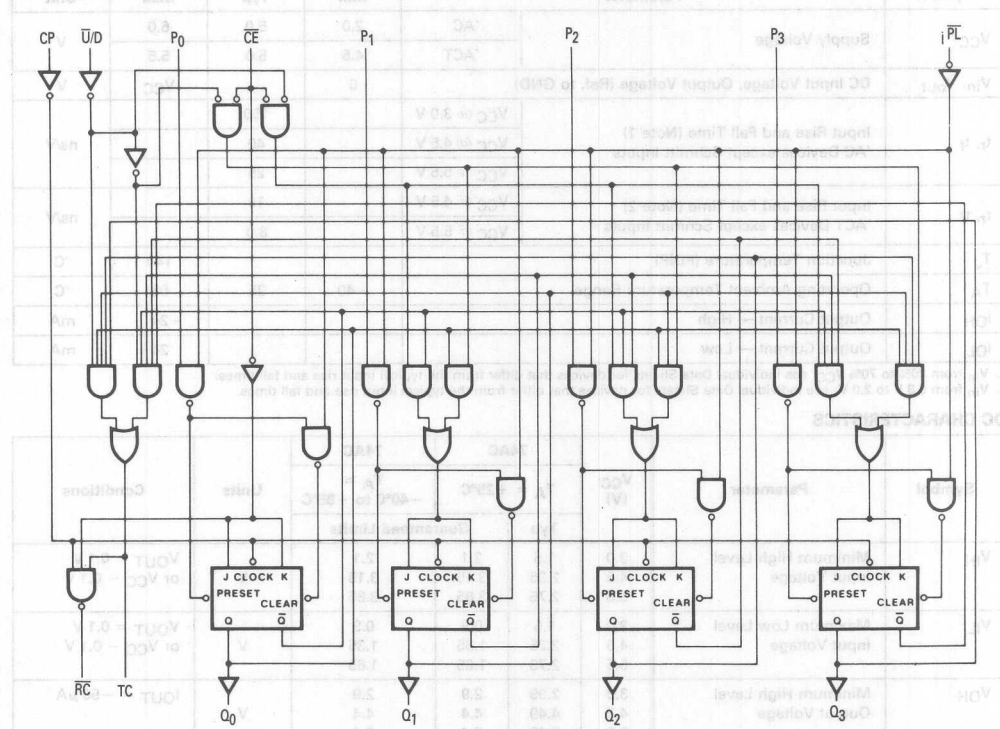


Figure c: Synchronous N-Stage Counter With Parallel Gated Carry/Borrow



MC74AC190

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of the logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

FACT DATA

MC74AC190

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} = -24 mA -24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC190

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC190			74AC190		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	80 110					MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	2.0 1.5		1.4 9.5	2.0 2.0	15.5 11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	2.5 1.5		14.5 10.0	2.0 2.0	16.0 11.5	ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	3.5 2.5		17.0 11.5	2.0 2.0	18.5 13.0	ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.5		17.0 12.5	2.0 2.0	18.5 13.0	ns	3-6
t _{PLH}	Propagation Delay CP to \overline{RC}	3.3 5.0	2.5 2.0		11.5 7.5	2.0 2.0	13.0 9.5	ns	3-6
t _{PHL}	Propagation Delay CP to \overline{RC}	3.3 5.0	2.5 1.5		11.0 8.0	2.0 2.0	12.5 9.5	ns	3-6
t _{PLH}	Propagation Delay \overline{CE} to \overline{RC}	3.3 5.0	2.5 1.5		12.0 8.0	2.0 2.0	13.0 9.0	ns	3-6
t _{PHL}	Propagation Delay \overline{CE} to \overline{RC}	3.3 5.0	2.0 1.5		13.0 8.0	2.0 2.0	14.5 9.0	ns	3-6
t _{PLH}	Propagation Delay $\overline{U/D}$ to \overline{RC}	3.3 5.0	2.5 1.5		14.0 8.5	2.0 2.0	15.5 10.0	ns	3-6
t _{PHL}	Propagation Delay $\overline{U/D}$ to \overline{RC}	3.3 5.0	2.5 2.5		13.0 8.5	2.0 2.0	14.5 10.0	ns	3-6
t _{PLH}	Propagation Delay $\overline{U/D}$ to TC	3.3 5.0	3.0 3.0		12.0 8.0	2.0 2.0	13.0 9.0	ns	3-6
t _{PHL}	Propagation Delay $\overline{U/D}$ to TC	3.3 5.0	3.0 3.0		12.0 8.0	2.0 2.0	13.0 9.0	ns	3-6
t _{PLH}	Propagation Delay P _n to Q _n	3.3 5.5	2.0 2.0		15.0 10.0	1.5 1.5	17.0 11.5	ns	3-6
t _{PHL}	Propagation Delay P _n to Q _n	3.3 5.0	2.0 2.0		14.0 9.5	1.5 1.5	16.0 11.0	ns	3-6
t _{PLH}	Propagation Delay \overline{PL} to Q _n	3.3 5.0	3.0 3.0		18.0 10.5	2.0 2.0	19.5 12.5	ns	3-6
t _{PHL}	Propagation Delay \overline{PL} to Q _n	3.3 5.0	2.5 2.0		15.0 10.5	2.0 2.0	17.0 12.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC190

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} [*] (V)	74AC190		74AC190		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum	Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW P _n to P _L	3.3 5.0	0.5 0	0.5 0	ns	3-9		
t _h	Hold Time, HIGH or LOW P _n to P _L	3.3 5.0	0 0	0 0	ns	3-9		
t _s	Setup Time, LOW C _E to C _P	3.3 5.0	6.5 4.5	7.5 5.0	ns	3-9		
t _h	Hold Time, LOW C _E to C _P	3.3 5.0	0 0	0 0	ns	3-9		
t _s	Setup Time, HIGH or LOW U/D to C _P	3.3 5.0	8.5 5.0	9.5 6.0	ns	3-9		
t _h	Hold Time, HIGH or LOW U/D to C _P	3.3 5.0	0 0	0 0	ns	3-9		
t _w	P _L Pulse Width, LOW	3.3 5.0	5.0 3.5	5.5 4.0	ns	3-6		
t _w	C _P Pulse Width, LOW	3.3 5.0	5.0 3.5	5.5 4.0	ns	3-6		
t _{rec}	Recovery Time P _L to C _P	3.3 5.0	0.5 0	0.5 0	ns	3-9		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	75	pF	V _{CC} = 5.0 V



MOTOROLA

**MC74AC194
MC74ACT194**

4-Bit Bidirectional Universal Shift Register

The MC74AC194/74ACT194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'AC/ACT194 is similar in operation to the 'AS195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- Typical Shift Frequency of 150 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers

FUNCTIONAL DESCRIPTION

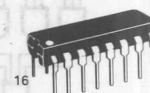
The MC74AC/74ACT194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0 , S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0 - P_3) and Serial data (DSR , DSL) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset (MR) overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

Operating Mode	Inputs					Outputs			
	MR	S ₁	S ₀	DSR	DSL	P _n	Q ₀	Q ₁	Q ₂ Q ₃
Reset	L	X	X	X	X	X	L	L	L L
Hold	H	I	I	X	X	X	q ₀	q ₁	q ₂ q ₃
Shift Left	H	h	I	X	I	X	q ₁	q ₂	q ₃ L
	H	h	I	X	h	X	q ₁	q ₂	q ₃ H
Shift Right	H	I	h	I	X	X	L	q ₀	q ₁ q ₂
	H	I	h	h	X	X	H	q ₀	q ₁ q ₂
Parallel Load	H	h	h	X	X	P _n	p ₀	p ₁	p ₂ p ₃

I = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
P_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

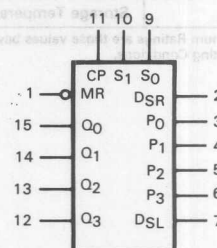
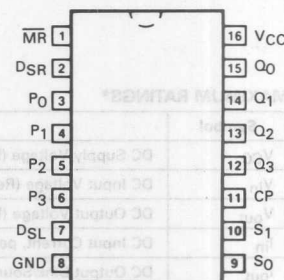
**4-BIT BIDIRECTIONAL
UNIVERSAL SHIFT
REGISTER**



**N SUFFIX
CASE 648-08
PLASTIC**

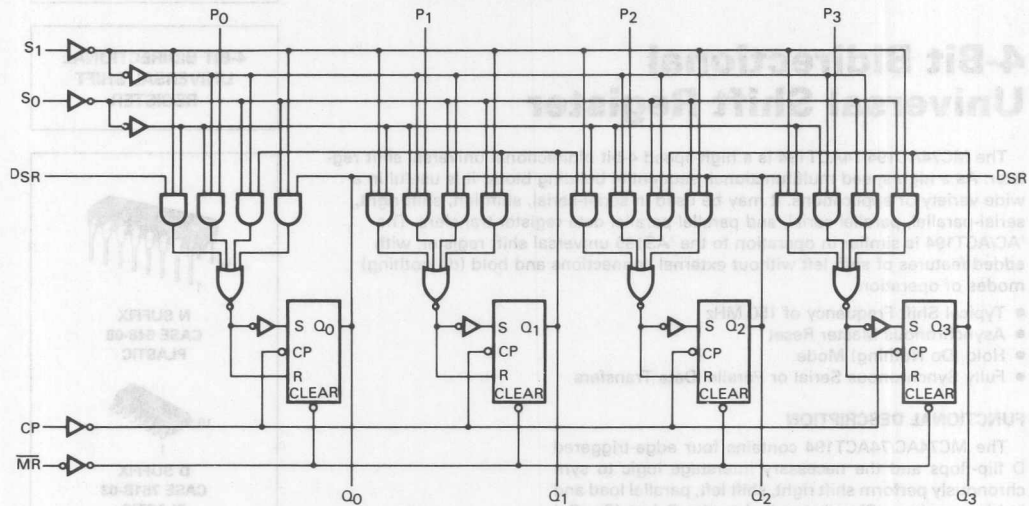


**D SUFFIX
CASE 751B-03
PLASTIC**



MC74AC194 • MC74ACT194

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC194 • MC74ACT194

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC 2.0	5.0	6.0	V
		'ACT 4.5	5.0	5.5	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC194 • MC74ACT194

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = -50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	3.3 5.0						MHz	3-3
t _{PLH}	Propagation Delay CP to Q	3.3 5.0		8.5 6.5				ns	3-6
t _{PHL}	Propagation Delay CP to Q	3.3 5.0		8.5 6.5				ns	3-6
t _{PHL}	Propagation Delay Reset to Q	3.3 5.0		7.5 5.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC194 • MC74ACT194

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0					ns	3-9
t _h	Hold Time, CP to any Input	3.3 5.0					ns	3-9
t _s	Setup Time, Parallel Data to CP	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW Data to CP	3.3 5.0					ns	3-9
t _w	CP Pulse Width	3.3 5.0	2.0 2.0	5.5 4.5	7.0 5.0		ns	3-6
t _w	MR Pulse Width	3.3 5.0	2.0 3.0	5.5 6.0	7.0 6.5		ns	3-9
t _{rec}	Recovery Time MR to CP	3.3 5.0	−2.5 −1.5	0 0	0 0		ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

			74ACT			74ACT			
Symbol	Parameter	V _{CC} * (V)	T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	5.0						MHz	3-3
t _{PLH}	Propagation Delay CP to Q	5.0						ns	3-6
t _{PHL}	Propagation Delay CP to Q	5.0						ns	3-6
t _{PHL}	Propagation Delay MR to Q	5.0		6.5	9.5	1.0	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC194 • MC74ACT194

AC OPERATING REQUIREMENTS

Symbol	Parameter	VCC* (V)	74ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum				
tS	Setup Time, HIGH or LOW S0 or S1 to CP	5.0					ns	3-9
tH	Hold Time, CP to any Input	5.0					ns	3-9
tS	Setup Time, Parallel Data to CP	5.0					ns	3-9
tH	Hold Time, HIGH or LOW Data to CP	5.0					ns	3-9
tW	CP Pulse Width HIGH or LOW	5.0					ns	3-9
tW	MR Pulse Width, LOW	5.0	5.5	8.5		9.5	ns	3-9
trec	Recovery Time MR to CP	5.0					ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance		pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance		pF	VCC = 5.0 V



MOTOROLA

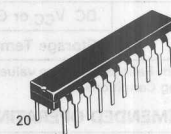
**MC74AC240
MC74ACT240**

Octal Buffer/Line Driver with 3-State Outputs

The MC74AC240/74ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT240 Has TTL Compatible Inputs

**OCTAL BUFFER/LINE
DRIVER WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**



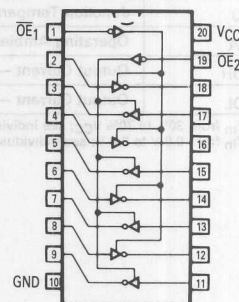
**DW SUFFIX
CASE 751D-03
PLASTIC**

TRUTH TABLES

Inputs		Outputs	
\overline{OE}_1	D	(Pins 12, 14, 16, 18)	
L	L	H	
L	H	L	
H	X	Z	

Inputs		Outputs	
\overline{OE}_2	D	(Pins 3, 5, 7, 9)	
L	L	H	
L	H	L	
H	X	Z	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



MC74AC240 • MC74ACT240

MAXIMUM RATINGS*

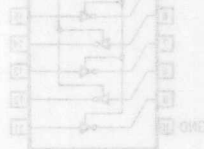
Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.



MC74AC240 • MC74ACT240

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC240 • MC74ACT240

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output	3.3 5.0	1.5 1.5	6.0 4.5	8.0 6.5	1.0 1.0	9.0 7.0	ns	3-5
t _{PHL}	Propagation Delay Data to Output	3.3 5.0	1.5 1.5	5.5 4.5	8.0 6.0	1.0 1.0	8.5 6.5	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	6.0 5.0	10.5 7.0	1.0 1.0	11.0 8.0	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	7.0 5.5	10.0 8.0	1.0 1.0	11.0 8.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	1.5 1.5	7.0 6.5	10.0 9.0	1.0 1.0	10.5 9.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	7.5 6.5	10.5 9.0	1.0 1.0	11.5 9.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output	5.0	1.5	6.0	8.5	1.5	9.5	ns	3-5
t _{PHL}	Propagation Delay Data to Output	5.0	1.5	5.5	7.5	1.5	8.5	ns	3-5
t _{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.0	9.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	2.0	8.0	9.5	2.0	10.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.5	6.5	10.0	2.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



MOTOROLA

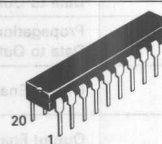
**MC74AC241
MC74ACT241**

Octal Buffer/Line Driver with 3-State Outputs

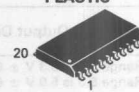
The MC74AC241/74ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT241 Has TTL Compatible Inputs

**OCTAL BUFFER/LINE
DRIVER WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**



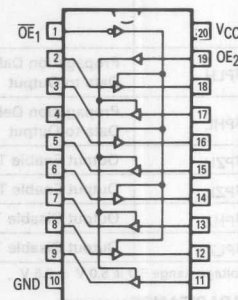
**DW SUFFIX
CASE 751D-03
PLASTIC**

TRUTH TABLES

Inputs		Outputs	
OE ₁	D	(Pins 12, 14, 16, 18)	
L	L	L	
L	H	H	
H	X	Z	

Inputs		Outputs	
OE ₂	D	(Pins 3, 5, 7, 9)	
H	L	L	
H	H	H	
L	X	Z	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5	19.0	19.5	20.0	20.5	21.0	21.5	22.0	22.5	23.0	23.5	24.0	24.5	25.0	25.5	26.0	26.5	27.0	27.5	28.0	28.5	29.0	29.5	30.0	30.5	31.0	31.5	32.0	32.5	33.0	33.5	34.0	34.5	35.0	35.5	36.0	36.5	37.0	37.5	38.0	38.5	39.0	39.5	40.0	40.5	41.0	41.5	42.0	42.5	43.0	43.5	44.0	44.5	45.0	45.5	46.0	46.5	47.0	47.5	48.0	48.5	49.0	49.5	50.0	50.5	51.0	51.5	52.0	52.5	53.0	53.5	54.0	54.5	55.0	55.5	56.0	56.5	57.0	57.5	58.0	58.5	59.0	59.5	60.0	60.5	61.0	61.5	62.0	62.5	63.0	63.5	64.0	64.5	65.0	65.5	66.0	66.5	67.0	67.5	68.0	68.5	69.0	69.5	70.0	70.5	71.0	71.5	72.0	72.5	73.0	73.5	74.0	74.5	75.0	75.5	76.0	76.5	77.0	77.5	78.0	78.5	79.0	79.5	80.0	80.5	81.0	81.5	82.0	82.5	83.0	83.5	84.0	84.5	85.0	85.5	86.0	86.5	87.0	87.5	88.0	88.5	89.0	89.5	90.0	90.5	91.0	91.5	92.0	92.5	93.0	93.5	94.0	94.5	95.0	95.5	96.0	96.5	97.0	97.5	98.0	98.5	99.0	99.5	100.0	100.5	101.0	101.5	102.0	102.5	103.0	103.5	104.0	104.5	105.0	105.5	106.0	106.5	107.0	107.5	108.0	108.5	109.0	109.5	110.0	110.5	111.0	111.5	112.0	112.5	113.0	113.5	114.0	114.5	115.0	115.5	116.0	116.5	117.0	117.5	118.0	118.5	119.0	119.5	120.0	120.5	121.0	121.5	122.0	122.5	123.0	123.5	124.0	124.5	125.0	125.5	126.0	126.5	127.0	127.5	128.0	128.5	129.0	129.5	130.0	130.5	131.0	131.5	132.0	132.5	133.0	133.5	134.0	134.5	135.0	135.5	136.0	136.5	137.0	137.5	138.0	138.5	139.0	139.5	140.0	140.5	141.0	141.5	142.0	142.5	143.0	143.5	144.0	144.5	145.0	145.5	146.0	146.5	147.0	147.5	148.0	148.5	149.0	149.5	150.0	150.5	151.0	151.5	152.0	152.5	153.0	153.5	154.0	154.5	155.0	155.5	156.0	156.5	157.0	157.5	158.0	158.5	159.0	159.5	160.0	160.5	161.0	161.5	162.0	162.5	163.0	163.5	164.0	164.5	165.0	165.5	166.0	166.5	167.0	167.5	168.0	168.5	169.0	169.5	170.0	170.5	171.0	171.5	172.0	172.5	173.0	173.5	174.0	174.5	175.0	175.5	176.0	176.5	177.0	177.5	178.0	178.5	179.0	179.5	180.0	180.5	181.0	181.5	182.0	182.5	183.0	183.5	184.0	184.5	185.0	185.5	186.0	186.5	187.0	187.5	188.0	188.5	189.0	189.5	190.0	190.5	191.0	191.5	192.0	192.5	193.0	193.5	194.0	194.5	195.0	195.5	196.0	196.5	197.0	197.5	198.0	198.5	199.0	199.5	200.0	200.5	201.0	201.5	202.0	202.5	203.0	203.5	204.0	204.5	205.0	205.5	206.0	206.5	207.0	207.5	208.0	208.5	209.0	209.5	210.0	210.5	211.0	211.5	212.0	212.5	213.0	213.5	214.0	214.5	215.0	215.5	216.0	216.5	217.0	217.5	218.0	218.5	219.0	219.5	220.0	220.5	221.0	221.5	222.0	222.5	223.0	223.5	224.0	224.5	225.0	225.5	226.0	226.5	227.0	227.5	228.0	228.5	229.0	229.5	230.0	230.5	231.0	231.5	232.0	232.5	233.0	233.5	234.0	234.5	235.0	235.5	236.0	236.5	237.0	237.5	238.0	238.5	239.0	239.5	240.0	240.5	241.0	241.5	242.0	242.5	243.0	243.5	244.0	244.5	245.0	245.5	246.0	246.5	247.0	247.5	248.0	248.5	249.0	249.5	250.0	250.5	251.0	251.5	252.0	252.5	253.0	253.5	254.0	254.5	255.0	255.5	256.0	256.5	257.0	257.5	258.0	258.5	259.0	259.5	260.0	260.5	261.0	261.5	262.0	262.5	263.0	263.5	264.0	264.5	265.0	265.5	266.0	266.5	267.0	267.5	268.0	268.5	269.0	269.5	270.0	270.5	271.0	271.5	272.0	272.5	273.0	273.5	274.0	274.5	275.0	275.5	276.0	276.5	277.0	277.5	278.0	278.5	279.0	279.5	280.0	280.5	281.0	281.5	282.0	282.5	283.0	283.5	284.0	284.5	285.0	285.5	286.0	286.5	287.0	287.5	288.0	288.5	289.0	289.5	290.0	290.5	291.0	291.5	292.0	292.5	293.0	293.5	294.0	294.5	295.0	295.5	296.0	296.5	297.0	297.5	298.0	298.5	299.0	299.5	300.0	300.5	301.0	301.5	302.0	302.5	303.0	303.5	304.0	304.5	305.0	305.5	306.0	306.5	307.0	307.5	308.0	308.5	309.0	309.5	310.0	310.5	311.0	311.5	312.0	312.5	313.0	313.5	314.0	314.5	315.0	315.5	316.0	316.5	317.0	317.5	318.0	318.5	319.0	319.5	320.0	320.5	321.0	321.5	322.0	322.5	323.0	323.5	324.0	324.5	325.0	325.5	326.0	326.5	327.0	327.5	328.0	328.5	329.0	329.5	330.0	330.5	331.0	331.5	332.0	332.5	333.0	333.5	334.0	334.5	335.0	335.5	336.0	336.5	337.0	337.5	338.0	338.5	339.0	339.5	340.0	340.5	341.0	341.5	342.0	342.5	343.0	343.5	344.0	344.5	345.0	345.5	346.0	346.5	347.0	347.5	348.0	348.5	349.0	349.5	350.0	350.5	351.0	351.5	352.0	352.5	353.0	353.5	354.0	354.5	355.0	355.5	356.0	356.5	357.0	357.5	358.0	358.5	359.0	359.5	360.0	360.5	361.0	361.5	362.0	362.5	363.0	363.5	364.0	364.5	365.0	365.5	366.0	366.5	367.0	367.5	368.0	368.5	369.0	369.5	370.0	370.5	371.0	371.5	372.0	372.5	373.0	373.5	374.0	374.5	375.0	375.5	376.0	376.5	377.0	377.5	378.0	378.5	379.0	379.5	380.0	380.5	381.0	381.5	382.0	382.5	383.0	383.5	384.0	384.5	385.0	385.5	386.0	386.5	387.0	387.5	388.0	388.5	389.0	389.5	390.0	390.5	391.0	391.5	392.0	392.5	393.0	393.5	394.0	394.5	395.0	395.5	396.0	396.5	397.0	397.5	398.0	398.5	399.0	399.5	400.0	400.5	401.0	401.5	402.0	402.5	403.0	403.5	404.0	404.5	405.0	405.5	406.0	406.5	407.0	407.5	408.0	408.5	409.0	409.5	410.0	410.5	411.0	411.5	412.0	412.5	413.0	413.5	414.0	414.5	415.0	415.5	416.0	416.5	417.0	417.5	418.0	418.5	419.0	419.5	420.0	420.5	421.0	421.5	422.0	422.5	423.0	423.5	424.0	424.5	425.0	425.5	426.0	426.5	427.0	427.5	428.0	428.5	429.0	429.5	430.0	430.5	431.0	431.5	432.0	432.5	433.0	433.5	434.0	434.5	435.0	435.5	436.0	436.5	437.0	437.5	438.0	438.5	439.0	439.5	440.0	440.5	441.0	441.5	442.0	442.5	443.0	443.5	444.0	444.5	445.0	445.5	446.0	446.5	447.0	447.5	448.0	448.5	449.0	449.5	450.0	450.5	451.0	451.5	452.0	452.5	453.0	453.5	454.0	454.5	455.0	455.5	456.0	456.5	457.0	457.5	458.0	458.5	459.0	459.5	460.0	460.5	461.0	461.5	462.0	462.5	463.0	463.5	464.0	464.5	465.0	465.5	466.0	466.5	467.0	467.5	468.0	468.5	469.0	469.5	470.0	470.5	471.0	471.5	472.0	472.5	473.0	473.5	474.0	474.5	475.0	475.5	476.0	476.5	477.0	477.5	478.0	478.5	479.0	479.5	480.0	480.5	481.0	481.5	482.0	482.5	483.0	483.5	484.0	484.5	485.0	485.5	486.0	486.5	487.0	487.5	488.0	488.5	489.0	489.5	490.0	490.5	491.0	491.5	492.0	492.5	493.0	493.5	494.0	494.5	495.0	495.5	496.0	496.5	497.0	497.5	498.0	498.5	499.0	499.5	500.0	500.5	501.0	501.5	502.0	502.5	503.0	503.5	504.0	504.5	505.0	505.5	506.0	506.5	507.0	507.5	508.0	508.5	509.0	509.5	510.0	510.5	511.0	511.5	512.0	512.5	513.0	513.5	514.0	514.5	515.0	515.5	516.0	516.5	517.0	517.5	518.0	518.5	519.0	519.5	520.0	520.5	521.0	521.5	522.0	522.5	523.0	523.5	524.0	524.5	525.0	525.5	526.0	526.5	527.0	527.5	528.0	528.5	529.0	529.5	530.0	530.5	531.0	531.5	532.0	532.5	533.0	533.5	534.0	534.5	535.0	535.5	536.0	536.5	537.0	537.5	538.0	538.5	539.0	539.5	540.0	540.5	541.0	541.5	542.0	542.5	543.0	543.5	544.0	544.5	545.0	545.5	546.0	546.5	547.0	547.5	548.0	548.5	549.0	549.5	550.0	550.5	551.0	551.5	552.0	552.5	553.0	553.5	554.0	554.5	555.0	555.5	556.0	556.5	557.0	557.5	558.0	558.5	559.0	559.5	560.0	560.5	561.0	561.5	562.0	562.5	563.0	563.5	564.0	564.5	565.0	565.5	566.0	566.5	567.0	567.5	568.0	568.5	569.0	569.5	570.0	570.5	571.0	571.5	572.0	572.5	573.0	573.5	574.0	574.5	575.0	575.5	576.0	576.5	577.0	577.5	578.0	578.5	579.0	579.5	580.0	580.5	581.0	581.5	582.0	582.5	583.0	583.5	584.0	584.5	585.0	585.5	586.0	586.5	587.0	587.5	588.0	588.5	589.0	589.5	590.0	590.5	591.0	591.5	592.0	592.5	593.0	593.5	594.0	594.5	595.0	595.5	596.0	596.5	597.0	597.5	598.0	598.5	599.0	599.5	600.0	600.5	601.0	601.5	602.0	602.5	603.0	603.5	604.0	604.5	605.0	605.5	606.0	606.5	607.0	607.5	608.0	608.5	609.0	609.5	610.0	610.5	611.0	611.5	612.0	612.5	613.0	613.5	614.0	614.5	615.0	615.5	616.0	616.5	617.0	617.5	618.0	618.5	619.0	619.5	620.0	620.5	621.0	621.5	622.0	622.5	623.0	623.5	624.0	624.5	625.0	625.5	626.0	626.5	627.0	627.5	628.0	628.5	629.0	629.5	630.0	630.5	63
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MC74AC241 • MC74ACT241

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC			74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay Data to Output	3.3 5.0	1.5 1.5	6.0 5.0	9.0 7.0	1.5 1.0	10.0 7.5	ns	3-5
tPHL	Propagation Delay Data to Output	3.3 5.0	1.5 1.5	6.0 4.5	9.0 7.0	1.0 1.0	10.5 7.5	ns	3-5
tPZH	Output Enable Time	3.3 5.0	1.5 1.5	6.5 5.5	12.5 9.0	1.0 1.0	13.0 9.5	ns	3-7
tPZL	Output Enable Time	3.3 5.0	1.5 1.5	7.0 5.5	12.0 9.0	1.5 1.0	13.0 9.5	ns	3-8
tPHZ	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.5	12.0 10.0	2.0 1.0	12.5 10.5	ns	3-7
tPLZ	Output Disable Time	3.3 5.0	1.5 1.5	7.0 6.0	12.5 10.0	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output	5.0	1.5	6.5	9.0	1.5	10.0	ns	3-5
t _{PHL}	Propagation Delay Data to Output	5.0	1.5	7.0	9.0	1.5	10.0	ns	3-5
t _{PZH}	Output Enable Time	5.0	1.5	6.0	9.0	1.0	10.0	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5	7.0	10.0	1.5	11.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5	8.0	10.5	1.5	11.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.0	7.0	10.5	1.5	11.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



MOTOROLA

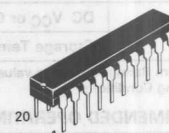
**MC74AC244
MC74ACT244**

Octal Buffer/Line Driver with 3-State Outputs

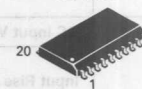
The MC74AC244/74ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT244 Has TTL Compatible Inputs

**OCTAL BUFFER/LINE
DRIVER WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**



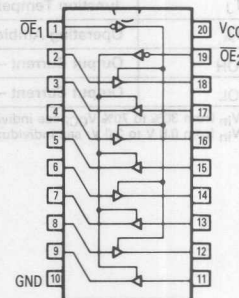
**DW SUFFIX
CASE 751D-03
PLASTIC**

TRUTH TABLES

Inputs		Outputs (Pins 12, 14, 16, 18)	
OE ₁	D		
L	L	L	
L	H	H	
H	X	Z	

Inputs		Outputs (Pins 3, 5, 7, 9)	
OE ₂	D		
L	L	L	
L	H	H	
H	X	Z	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



MC74AC244 • MC74ACT244

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	150		ns/V
		$V_{CC} @ 4.5 V$	40		
		$V_{CC} @ 5.5 V$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	10		ns/V
		$V_{CC} @ 5.5 V$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC244 • MC74ACT244

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
	V	3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
	V	3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC244 • MC74ACT244

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GN} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC244 • MC74ACT244

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	6.5 5.0	9.0 7.0	1.5 1.0	10.0 7.5	ns	3-5
t _{PHL}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	6.5 5.0	9.0 7.0	2.0 1.0	10.0 7.5	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	2.0 1.5	6.0 5.0	10.5 7.0	1.5 1.5	11.0 8.0	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 1.5	7.5 5.5	10.0 8.0	2.0 1.5	11.0 8.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	3.0 2.5	7.0 6.5	10.0 9.0	1.5 1.0	10.5 9.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.5 2.0	7.5 6.5	10.5 9.0	2.5 2.0	11.5 9.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output	5.0	2.0	6.5	9.0	1.5	10.0	ns	3-5
t _{PHL}	Propagation Delay Data to Output	5.0	2.0	7.0	9.0	1.5	10.0	ns	3-5
t _{PZH}	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.5	7.5	10.0	2.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



MOTOROLA

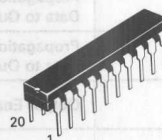
**MC74AC245
MC74ACT245**

Octal Bidirectional Transceiver with 3-State Inputs/Outputs

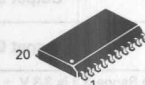
The MC74AC245/74ACT245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

- Noninverting Buffers
- Bidirectional Data Path
- A and B Outputs Source/Sink 24 mA
- 'ACT245 Has TTL Compatible Inputs

**OCTAL BIDIRECTIONAL
TRANSCIVER
WITH 3-STATE
INPUTS/OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**

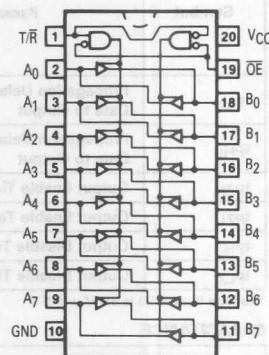
PIN NAMES

OE Output Enable Input
T/R Transmit/Receive Input
A₀-A₇ Side A 3-State Inputs or 3-State Outputs
B₀-B₇ Side B 3-State Inputs or 3-State Outputs

TRUTH TABLES

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



FACT DATA

MC74AC245 • MC74ACT245

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC245 • MC74ACT245

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

Symbol	Parameter	V _{IN} Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{OP}	Output Capacitance	18	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V

FACT DATA

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC			74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay An to Bn or Bn to An	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.5	1.0 1.0	9.0 7.0	ns	3-5
tPHL	Propagation Delay An to Bn or Bn to An	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.0	1.0 1.0	9.0 7.0	ns	3-5
tPZH	Output Enable Time	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	2.0 1.0	12.5 9.0	ns	3-7
tPZL	Output Enable Time	3.3 5.0	2.5 1.5	7.5 5.5	12.0 9.0	2.0 1.0	13.5 9.5	ns	3-8
tPHZ	Output Disable Time	3.3 5.0	2.0 1.5	6.5 5.5	12.0 9.0	1.0 1.0	12.5 10.0	ns	3-7
tPLZ	Output Disable Time	3.3 5.0	2.0 1.5	7.0 5.5	11.5 9.0	1.5 1.0	13.0 10.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	5.0	1.5	4.0	7.5	1.5	8.0	ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	5.0	1.5	4.0	8.0	1.0	9.0	ns	3-5
t _{PZH}	Output Enable Time	5.0	1.5	5.0	10	1.5	11.0	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5	5.5	10	1.5	12.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5	5.5	10	1.0	11.0	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.0	5.0	10	1.5	11.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{I/N}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



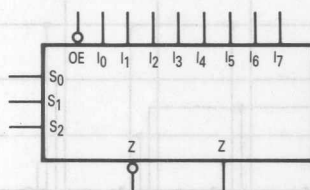
MOTOROLA

8-Input Multiplexer with 3-State Outputs

The MC74AC251/74ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

- Multifunctional Capability
- On-Chip Select Logic Decoding
- Inverting and Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT251 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

- S₀-S₂ Select Inputs
 OE 3-State Output Enable Input
 I₀-I₇ Multiplexer Inputs
 Z 3-State Multiplexer Output
 Z-bar Complementary 3-State Multiplexer Output

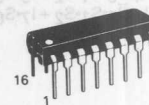
TRUTH TABLE

Inputs				Outputs	
OE	S ₂	S ₁	S ₀	Z	Z
H	X	X	X	Z	Z
L	L	L	L	I ₀	I ₀
L	L	L	H	I ₁	I ₁
L	L	H	L	I ₂	I ₂
L	L	H	H	I ₃	I ₃
L	H	L	L	I ₄	I ₄
L	H	L	H	I ₅	I ₅
L	H	H	L	I ₆	I ₆
L	H	H	H	I ₇	I ₇

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

**MC74AC251
MC74ACT251**

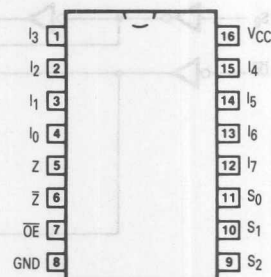
**8-INPUT
MULTIPLEXER WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**





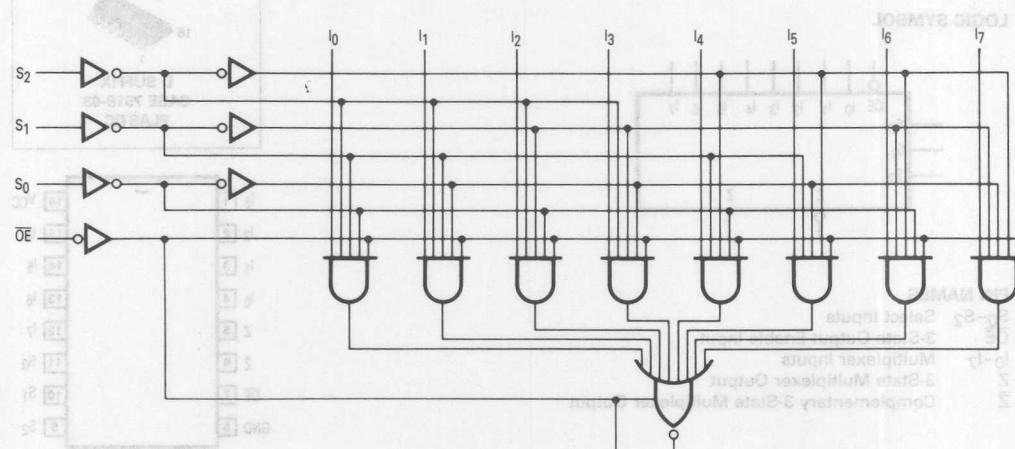
FUNCTIONAL DESCRIPTION

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both true and complementary outputs are provided. The Output Enable input (\overline{OE}) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot S_0 \cdot S_1 \cdot S_2 + I_1 \cdot S_0 \cdot S_1 \cdot S_2 + I_2 \cdot S_0 \cdot S_1 \cdot S_2 + I_3 \cdot S_0 \cdot S_1 \cdot S_2 + I_4 \cdot S_0 \cdot S_1 \cdot S_2 + I_5 \cdot S_0 \cdot S_1 \cdot S_2 + I_6 \cdot S_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TRUTH TABLE

Inputs	S_2	S_1	S_0	\overline{OE}	Z	\overline{Z}
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	0	1
3	0	1	1	0	1	0
4	1	0	0	0	0	1
5	1	0	1	0	1	0
6	1	1	0	0	0	1
7	1	1	1	0	1	0
8	X	X	X	1	X	X

H = HIGH Voltage Level
L = LOW Voltage Level
X = Indifferent
Z = High Impedance

MC74AC251 • MC74ACT251

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0	V _{CC}	V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions	
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA	
		4.5		3.86	3.76			I _{OH} –24 mA
		5.5		4.86	4.76			–24 mA
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA	
		4.5		0.36	0.44			I _{OL} 24 mA
		5.5		0.36	0.44			24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = -50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _N to Z or Z̄	3.3 5.0	1.5 1.5	11.5 8.5	17.5 12.5	1.5 1.5	19.0 13.5	ns	3-6
t _{PHL}	Propagation Delay S _N to Z or Z̄	3.3 5.0	1.5 1.5	11.0 8.0	17.5 12.5	1.5 1.5	19.0 13.5	ns	3-6
t _{PLH}	Propagation Delay I _N to Z or Z̄	3.3 5.0	1.5 1.5	10.0 7.0	14.0 10.0	1.5 1.5	15.5 11.0	ns	3-5
t _{PHL}	Propagation Delay I _N to Z or Z̄	3.3 5.0	1.5 1.5	9.0 6.5	14.0 10.0	1.5 1.5	15.5 11.0	ns	3-5
t _{PZH}	Output Enable Time OE to Z or Z̄	3.3 5.0	1.5 1.5	7.5 5.5	11.0 8.0	1.5 1.5	12.0 9.0	ns	3-7
t _{PZL}	Output Enable Time OE to Z or Z̄	3.3 5.0	1.5 1.5	7.5 5.5	11.0 8.0	1.5 1.5	12.0 9.0	ns	3-8
t _{PHZ}	Output Disable Time OE to Z or Z̄	3.3 5.0	1.5 1.5	8.5 7.0	11.5 9.5	1.5 1.5	13.0 10.0	ns	3-7
t _{PLZ}	Output Disable Time OE to Z or Z̄	3.3 5.0	1.5 1.5	7.0 5.5	11.0 8.0	1.5 1.5	12.0 8.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC251 • MC74ACT251

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z or Z	5.0	2.5	7.0	15.5	2.0	17.0	ns	3-6
t _{PHL}	Propagation Delay S _n to Z or Z	5.0	2.5	7.5	16.5	2.5	18.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z or Z	5.0	2.5	5.5	12.0	2.0	13.0	ns	3-5
t _{PHL}	Propagation Delay I _n to Z or Z	5.0	2.5	6.5	12.5	2.5	14.0	ns	3-5
t _{PZH}	Output Enable Time OE to Z or Z	5.0	1.5	5.0	8.5	1.5	9.0	ns	3-7
t _{PZL}	Output Enable Time OE to Z or Z	5.0	1.5	4.5	8.5	1.5	9.0	ns	3-8
t _{PHZ}	Output Disable Time OE to Z or Z	5.0	2.0	6.0	12.0	2.0	13.0	ns	3-7
t _{PLZ}	Output Disable Time OE to Z or Z	5.0	3.0	4.5	8.5	3.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	70	pF	VCC = 5.0 V

Symbol	Parameter	VCC* (V)	TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay Sn to Z or Z	5.0	2.5	7.0	15.5	2.0	17.0	ns	3-6
tPHL	Propagation Delay Sn to Z or Z	5.0	2.5	7.5	16.5	2.5	18.5	ns	3-6
tPLH	Propagation Delay In to Z or Z	5.0	2.5	5.5	12.0	2.0	13.0	ns	3-5
tPHL	Propagation Delay In to Z or Z	5.0	2.5	6.5	12.5	2.5	14.0	ns	3-5
tPZH	Output Enable Time OE to Z or Z	5.0	1.5	5.0	8.5	1.5	9.0	ns	3-7
tPZL	Output Enable Time OE to Z or Z	5.0	1.5	4.5	8.5	1.5	9.0	ns	3-8
tPHZ	Output Disable Time OE to Z or Z	5.0	2.0	6.0	12.0	2.0	13.0	ns	3-7
tPLZ	Output Disable Time OE to Z or Z	5.0	3.0	4.5	8.5	3.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA



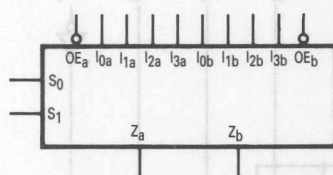
MOTOROLA

Dual 4-Input Multiplexer with 3-State Outputs

The MC74AC253/74ACT253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (\overline{OE}) inputs, allowing the outputs to interface directly with bus oriented systems.

- Multifunctional Capability
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT253 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

- $I_{0a}-I_{3a}$ Side A Data Inputs
- $I_{0b}-I_{3b}$ Side B Data Inputs
- S_0, S_1 Common Select Inputs
- \overline{OE}_a Side A Output Enable Input
- \overline{OE}_b Side B Output Enable Input
- Z_a, Z_b 3-State Outputs

TRUTH TABLE

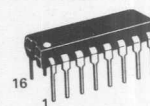
Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	\overline{OE}	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

MC74AC253
MC74ACT253

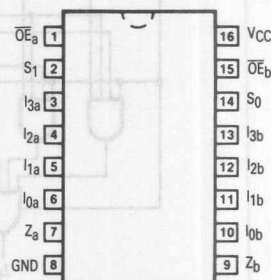
DUAL 4-INPUT
MULTIPLEXER WITH
3-STATE OUTPUTS



N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC



MC74AC253 • MC74ACT253

FUNCTIONAL DESCRIPTION

The MC74AC253/74ACT253 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a, \overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic

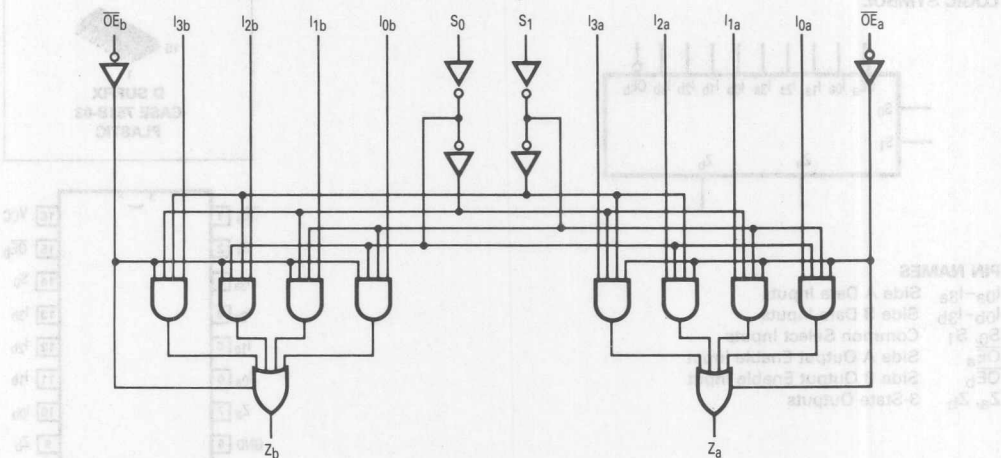
equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Table		Select Inputs				Data Inputs				Outputs	
S_1	S_0	I_0	I_1	I_2	I_3	Z_0	Z_1	Z_2	Z_3	Z_0	Z_1
0	0	X	X	X	X	X	X	X	X	X	X
0	1	X	X	X	X	X	X	X	X	X	X
1	0	X	X	X	X	X	X	X	X	X	X
1	1	X	X	X	X	X	X	X	X	X	X

FACT DATA

MC74AC253 • MC74ACT253

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	− 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	− 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	150		ns/V
		$V_{CC} @ 4.5 V$	40		
		$V_{CC} @ 5.5 V$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	10		ns/V
		$V_{CC} @ 5.5 V$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	− 40	25	85	°C
I_{OH}	Output Current — High			− 24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC253 • MC74ACT253

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC253 • MC74ACT253

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	3.3 5.0	2.0 2.0		15.5 11.0	2.0 1.5	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay S _n to Z _n	3.3 5.0	2.5 2.0		16.0 11.5	2.0 1.5	18.0 13.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5		14.5 10.0	1.5 1.5	17.0 11.5	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	2.0 1.5		13.0 9.5	1.5 1.5	15.0 11.0	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5		8.0 6.0	1.0 1.0	8.5 6.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5		8.0 6.0	1.0 1.0	9.0 7.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	2.0 2.0		9.5 8.0	1.5 1.5	10.0 8.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5		8.0 7.0	1.0 1.0	9.0 7.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC253 • MC74ACT253

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _N to Z _N	5.0	2.0		11.5	2.0	13.0	ns	3-6
t _{PHL}	Propagation Delay S _N to Z _N	5.0	3.0		13.0	2.5	14.5	ns	3-6
t _{PLH}	Propagation Delay I _N to Z _N	5.0	2.5		10.0	2.0	11.0	ns	3-5
t _{PHL}	Propagation Delay I _N to Z _N	5.0	3.5		11.0	3.0	12.5	ns	3-5
t _{PZH}	Output Enable Time	5.0	2.0		7.5	1.5	8.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0		8.0	1.5	9.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	3.0		9.5	2.5	10.0	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.5		7.5	2.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF V _{CC} = 5.0 V



MOTOROLA

**MC74AC256
MC74ACT256**

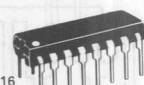
Dual 4-Bit Addressable Latch

The MC74AC256/74ACT256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

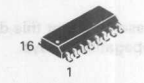
In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode (MR = \bar{E} = LOW), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

- Combines Dual Demultiplexer and 8-Bit Latch
- Serial-to-Parallel Capability
- Output from Each Storage Bit Available
- Random (Addressable) Data Entry
- Easily Expandable
- Common Clear Input
- Useful as Dual 1-of-4 Active HIGH Decoder

**DUAL 4-BIT
ADDRESSABLE
LATCH**

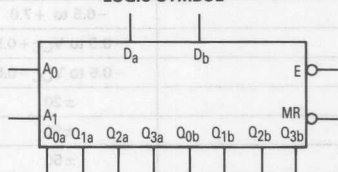


**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**

LOGIC SYMBOL



MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs						Outputs			
	MR	\bar{E}	D	A ₀	A ₁		Q ₀	Q ₁	Q ₂	Q ₃
Master Reset	L	H	X	X	X		L	L	L	L
Demultiplex (Active HIGH Decoder when D=H)	L	L	d	L	L		Q=d	L	L	L
	L	L	d	H	L		L	Q=d	L	L
	L	L	d	L	H		L	L	Q=d	L
	L	L	d	H	H		L	L	L	Q=d
Store (Do Nothing)	H	H	X	X	X		q ₀	q ₁	q ₂	q ₃
Addressable Latch	H	L	d	L	L		Q=d	q ₁	q ₂	q ₃
	H	L	d	H	L		q ₀	Q=d	q ₂	q ₃
	H	L	d	L	H		q ₀	q ₁	Q=d	q ₃
	H	L	d	H	H		q ₀	q ₁	q ₂	Q=d

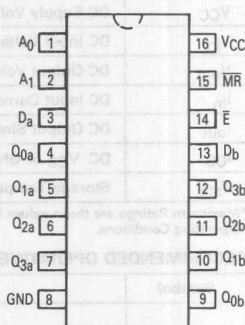
H = HIGH Voltage Level Steady State

L = LOW Voltage Level Steady State

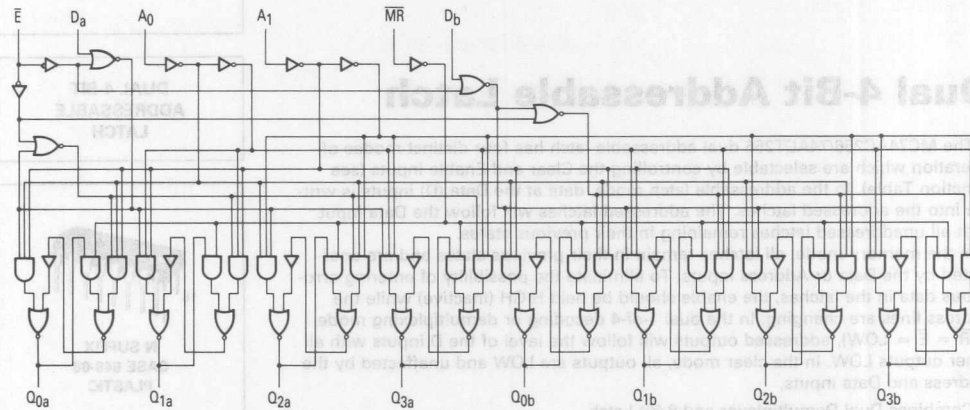
X = Immaterial

d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	V_{AC}	2.0	5.0	V
		V_{ACT}	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	150		ns/V
		$V_{CC} @ 4.5 V$	40		
		$V_{CC} @ 5.5 V$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	10		ns/V
		$V_{CC} @ 5.5 V$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

- V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

FACT DATA

MC74AC256 • MC74ACT256

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
	V _{IH}	3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC256 • MC74ACT256

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
		5.5		4.86	4.76			
		V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V
5.5	0.001			0.1	0.1			
4.5				0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
5.5				0.36	0.44			
I _{IN}	Maximum Input Leakage Current			5.5		±0.1	±1.0	μA
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC256 • MC74ACT256

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _N to Q _N	3.3 5.0	2.0 2.0	9.0 6.5	14.5 10.0	1.5 1.5	17.0 11.5	ns	3-5
t _{PHL}	Propagation Delay D _N to Q _N	3.3 5.0	2.0 2.0	9.0 6.0	13.5 9.5	1.5 1.5	16.0 11.0	ns	3-5
t _{PLH}	Propagation Delay E to Q _N	3.3 5.0	2.0 2.0	10.5 7.0	15.0 10.5	1.5 1.5	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay E to Q _N	3.3 5.0	2.0 2.0	8.0 7.5	12.5 9.0	1.5 1.5	15.0 11.0	ns	3-6
t _{PLH}	Propagation Delay Address to Q _N	3.3 5.0	2.0 2.0	12.0 8.0	19.0 13.0	1.5 1.5	22.5 15.5	ns	3-6
t _{PHL}	Propagation Delay Address to Q _N	3.3 5.0	2.0 2.0	10.0 7.0	16.0 11.0	1.5 1.5	19.0 13.0	ns	3-6
t _{PHL}	Propagation Delay MR to Q	3.3 5.0	2.0 2.0	8.0 6.0	12.0 9.0	1.5 1.5	13.5 10.0	ns	3-7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _N to \bar{E}	3.3 5.0		3.5 2.5	4.5 3.5	ns	3-9
t _h	Hold Time, HIGH or LOW D _N to \bar{E}	3.3 5.0		2.5 2.0	2.5 2.0	ns	3-9
t _s	Setup Time Address to \bar{E}	3.3 5.0		7.0 4.0	9.0 6.0	ns	3-6
t _h	Hold Time Address to \bar{E}	3.3 5.0		2.0 2.0	2.0 2.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	Units	Test Conditions
C _{IN}	Input Capacitance	pf	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	pf	V _{CC} = 5.0 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _N to Q _N	5.0	2.0	6.5	11.5	1.5	13.0	ns	3-5
t _{PHL}	Propagation Delay D _N to Q _N	5.0	2.0	7.0	11.0	1.5	12.5	ns	3-5
t _{PLH}	Propagation Delay E̅ to Q _N	5.0	2.0	8.0	12.0	1.5	14.0	ns	3-6
t _{PHL}	Propagation Delay E̅ to Q _N	5.0	2.0	6.5	10.5	1.5	12.5	ns	3-6
t _{PLH}	Propagation Delay Address to Q _N	5.0	2.0	10.5	14.5	1.5	17.0	ns	3-6
t _{PHL}	Propagation Delay Address to Q _N	5.0	2.0	9.0	12.5	1.5	14.5	ns	3-6
t _{PHL}	Propagation Delay MR to Q	5.0	2.0	7.0	10.5	1.5	11.5	ns	3-7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to E	5.0		3.5	4.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to E	5.0		2.5	2.5	ns	3-9	
t _s	Setup Time Address to E	5.0		5.5	6.5	ns	3-6	
t _h	Hold Time Address to E	5.0		2.5	2.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	30.0	pF	VCC = 5.0 V



MOTOROLA

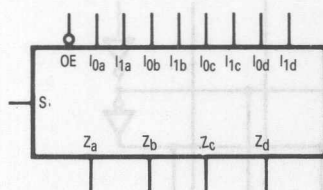
MC74AC257 MC74ACT257

Quad 2-Input Multiplexer with 3-State Outputs

The MC74AC257/74ACT257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT257 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

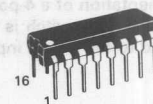
S Common Data Select Input
 \overline{OE} 3-State Output Enable Input
 I0a-I0d Data Inputs from Source 0
 I1a-I1d Data Inputs from Source 1
 Za-Zd 3-State Multiplexer Outputs

TRUTH TABLE

Output Enable	Select Input	Data Inputs		Outputs
\overline{OE}	S	I0	I1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

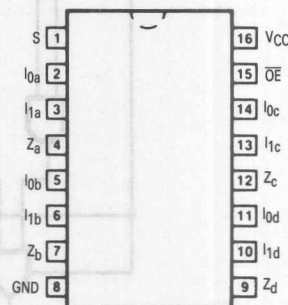
QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS



N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC



MC74AC257 • MC74ACT257



FUNCTIONAL DESCRIPTION

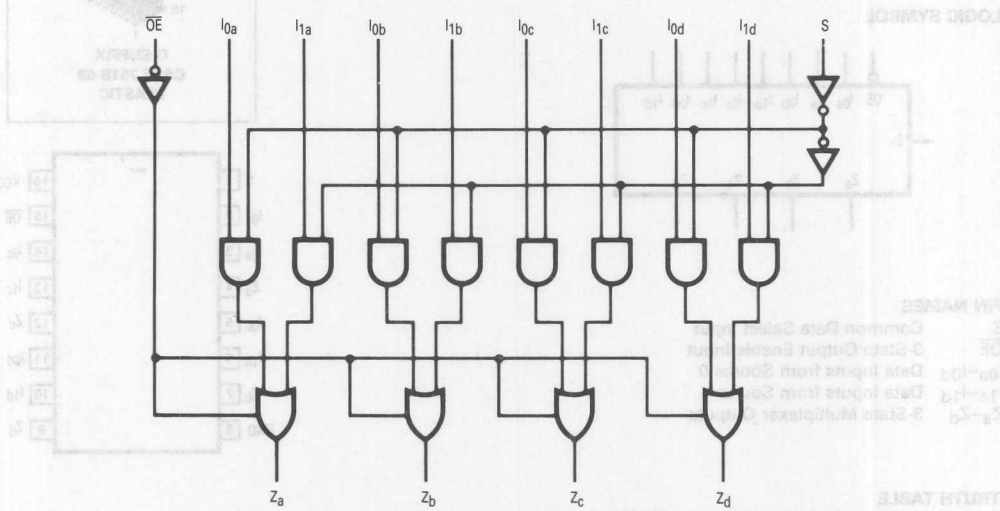
The MC74AC257/74ACT257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the

outputs are shown below:

$$\begin{aligned} Z_a &= \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \\ Z_b &= \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S}) \\ Z_c &= \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \\ Z_d &= \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S}) \end{aligned}$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Output Enable	Select Input	Data Input 1	Data Input 0	Output
H	X	X	X	X
L	X	X	L	L
L	X	H	H	H
L	L	L	L	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Indifferent
Z = High Impedance

MC74AC257 • MC74ACT257

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC257 • MC74ACT257

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC257 • MC74ACT257

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay I _N to Z _N	3.3 5.0	1.5 1.5	5.0 4.0	8.5 6.0	1.0 1.0	9.0 7.0	ns	3-5
t _{PHL}	Propagation Delay I _N to Z _N	3.3 5.0	1.5 1.5	6.0 4.5	8.5 6.0	1.0 1.0	9.0 7.0	ns	3-5
t _{PLH}	Propagation Delay S to Z _N	3.3 5.0	1.5 1.5	7.0 5.0	10.5 7.5	1.5 1.0	11.5 8.5	ns	3-6
t _{PHL}	Propagation Delay S to Z _N	3.3 5.0	1.5 1.5	7.5 5.5	10.5 7.5	1.5 1.0	11.5 8.5	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	6.5 5.0	9.5 7.5	1.0 1.0	10.5 8.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	5.5 5.0	9.0 8.5	1.0 1.0	10.0 9.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	1.5 1.5	5.5 5.0	10.0 9.0	1.0 1.0	11.0 10.0	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	5.5 5.0	9.0 8.0	1.0 1.0	10.0 9.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC257 • MC74ACT257

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay I _N to Z _N	5.0	1.5	5.0	7.0	1.0	7.5	ns	3-6
t _{PHL}	Propagation Delay I _N to Z _N	5.0	2.0	6.0	7.5	1.5	8.5	ns	3-6
t _{PLH}	Propagation Delay S to Z _N	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-6
t _{PHL}	Propagation Delay S to Z _N	5.0	2.5	7.0	10.5	2.0	11.5	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.0	6.0	8.0	1.5	9.0	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0	6.0	8.0	1.5	9.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	2.5	6.5	9.0	1.5	10.0	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.0	6.0	7.5	1.5	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V



MOTOROLA

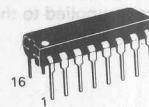
MC74AC258 MC74ACT258

Quad 2-Input Multiplexer with 3-State Outputs

The MC74AC258/74ACT258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Inverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT258 Has TTL Compatible Inputs

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

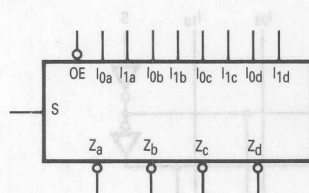


**N SUFFIX
CASE 648-08
PLASTIC**



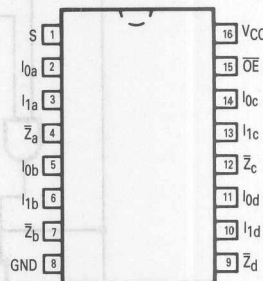
**D SUFFIX
CASE 751B-03
PLASTIC**

LOGIC SYMBOL



PIN NAMES

S	Common Data Select Input
\overline{OE}	3-State Output Enable Input
$I_{0a}-I_{0d}$	Data Inputs from Source 0
$I_{1a}-I_{1d}$	Data Inputs from Source 1
Z_a-Z_d	3-State Multiplexer Outputs



TRUTH TABLE

Output Enable	Select Input	Data Inputs		Outputs
\overline{OE}	S	I_0	I_1	\bar{Z}
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

MC74AC258 • MC74ACT258

FUNCTIONAL DESCRIPTION

The MC74AC258/74ACT258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The MC74AC258/74ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

tions for the outputs are shown below:

$$Z_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

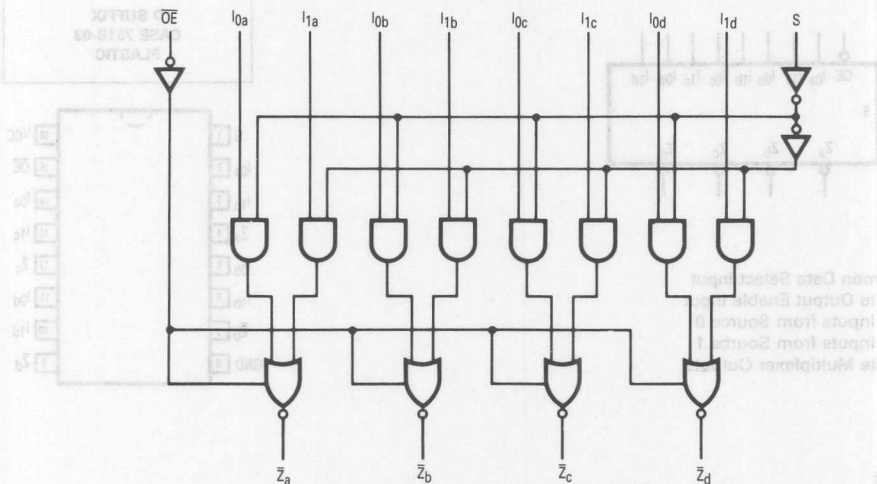
$$Z_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$Z_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Output Enable	Select	Data Input	Output
H	X	X	X
L	X	L	L
L	H	X	X
L	L	L	L
L	X	X	X
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Indifferent
Z = High Impedance

FACT DATA

MC74AC258 • MC74ACT258

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

V _{in} = V _{CC} or GND	I _{CC}	Supply Current	Maximum	Quiescent	50	mA
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MC74AC258 • MC74ACT258

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC258 • MC74ACT258

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

3-8	ns	8.8	1.8	8.8	8.8	3.0	8.8	8.8	Propagation Delay t _{PLH} 10 to 50%
3-8	ns	8.8	1.8	8.8	8.8	3.0	8.8	8.8	Propagation Delay t _{PLL} 10 to 50%
3-8	ns	11.2	3.0	10.8	1.8	3.0	8.8	8.8	Propagation Delay t _{PLH} 50 to 90%
3-8	ns	11.0	1.8	8.8	1.8	8.8	8.8	8.8	Propagation Delay t _{PLL} 50 to 90%
3-7	ns	8.8	1.8	8.8	8.8	3.0	8.8	8.8	Output Enable Time t _{ON}
3-8	ns	8.8	1.8	8.8	8.8	3.0	8.8	8.8	Output Enable Time t _{OFF}
3-7	ns	10.0	1.8	8.8	8.8	1.8	8.8	8.8	Output Disable Time t _{ON}
3-8	ns	9.0	1.8	8.8	8.8	3.0	8.8	8.8	Output Disable Time t _{OFF}

*Voltage range 4.5 to 5.5 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Units	Test Conditions
C _{IN}	Input Capacitance	pF	V _{CC} = 5.0 V
C _{OP}	Power Dissipation Capacitance	pF	V _{CC} = 5.0 V

MC74AC258 • MC74ACT258

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC			74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay In to Zn	3.3 5.0	2.0 1.5	6.0 4.5	9.5 7.5	1.5 1.0	11.0 8.5	ns	3-5
tPHL	Propagation Delay In to Zn	3.3 5.0	2.0 1.5	5.0 4.0	8.5 6.5	1.5 1.0	9.5 7.0	ns	3-5
tPLH	Propagation Delay S to Zn	3.3 5.0	3.0 2.0	7.5 6.0	12.0 9.5	2.5 1.5	14.0 10.5	ns	3-6
tPHL	Propagation Delay S to Zn	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.0	2.0 1.5	13.0 10.0	ns	3-6
tPZH	Output Enable Time	3.3 5.0	2.5 1.5	6.0 4.5	9.5 7.5	2.0 1.5	10.5 8.5	ns	3-7
tPZL	Output Enable Time	3.3 5.0	2.0 1.5	5.5 5.5	9.0 7.0	1.5 1.0	10.0 8.0	ns	3-8
tPHZ	Output Disable Time	3.3 5.0	2.5 2.0	5.5 5.5	10.0 8.5	2.0 1.5	11.5 9.0	ns	3-7
tPLZ	Output Disable Time	3.3 5.0	2.0 1.5	5.5 5.0	9.0 7.0	2.0 1.5	10.0 8.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay I _N to \bar{Z}_N	5.0	2.0	6.5	8.5	1.5	9.5	ns	3-5
t _{PHL}	Propagation Delay I _N to \bar{Z}_N	5.0	2.0	5.5	7.5	1.5	8.0	ns	3-5
t _{PLH}	Propagation Delay S to \bar{Z}_N	5.0	3.0	7.5	10.5	2.0	11.5	ns	3-6
t _{PHL}	Propagation Delay S to \bar{Z}_N	5.0	1.5	7.0	9.5	1.5	11.0	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.0	6.5	8.5	1.5	9.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0	6.5	8.5	1.5	9.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5	7.0	9.0	1.0	10.0	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.0	6.0	8.0	1.5	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	55	pF	VCC = 5.0 V



MOTOROLA

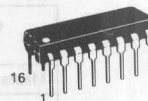
MC74AC259 MC74ACT259

8-Bit Addressable Latch

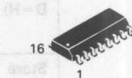
The MC74AC259/74ACT259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the ALS259 8-bit addressable latch.

- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

**8-BIT
ADDRESSABLE
LATCH**



**N SUFFIX
CASE 648-08
PLASTIC**

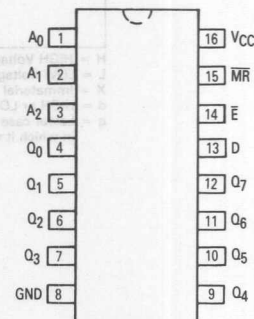


**D SUFFIX
CASE 751B-03
PLASTIC**

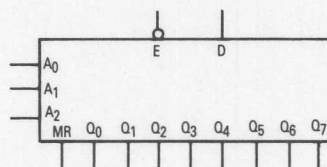
FUNCTIONAL DESCRIPTION

The MC74AC259/74ACT259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC74AC/ACT259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the MC74AC/ACT259.



LOGIC SYMBOL



FACT DATA

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MODE SELECT TABLE

\bar{E}	MR	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

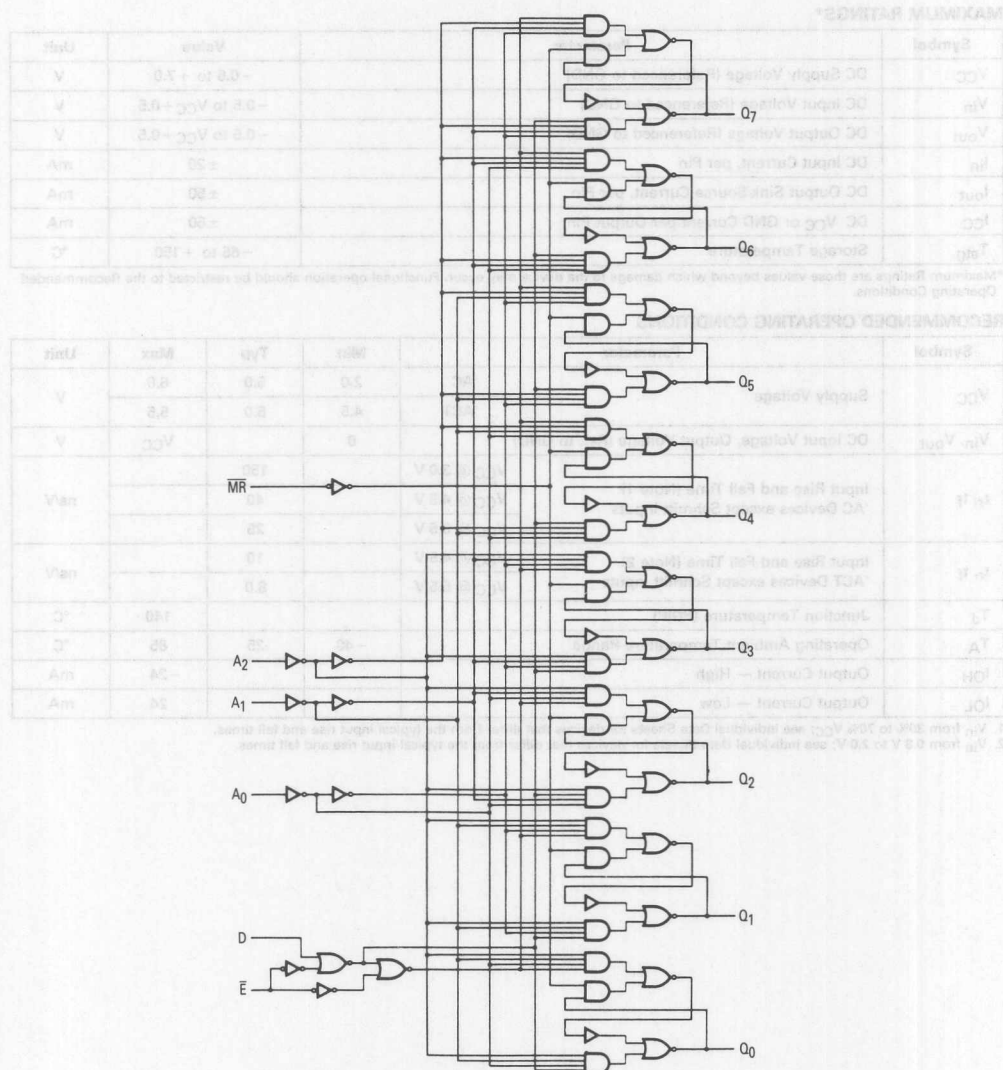
H = HIGH Voltage Level
L = LOW Voltage Level

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs														
	MR	\bar{E}	D	A ₀	A ₁	A ₂		Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Master Reset	L	H	X	X	X	X		L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	L	Q = d	L	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q = d	L	L	L	L
Store (Do Nothing)	H	H	X	X	X	X		q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable Latch	H	L	d	L	L	L	Q = d	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀ Q = d	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀ Q = d	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	H	L	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇	Q = d

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 \text{ V}$	150		ns/V
		$V_{CC} @ 4.5 \text{ V}$	40		
		$V_{CC} @ 5.5 \text{ V}$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 \text{ V}$	10		ns/V
		$V_{CC} @ 5.5 \text{ V}$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
	I _{OH}	3.0	1.0	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA −24 mA −24 mA	
		4.5	1.0	3.86	3.76			
		5.5	1.0	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
	I _{OL}	3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _N to Q _N	3.3 5.0	2.0 2.0	9.0 6.5	14.5 10.0	1.5 1.5	17.0 11.5	ns	3-5
t _{PHL}	Propagation Delay D _N to Q _N	3.3 5.0	2.0 2.0	9.0 6.0	13.5 9.5	1.5 1.5	16.0 11.0	ns	3-5
t _{PLH}	Propagation Delay E to Q _N	3.3 5.0	2.0 2.0	10.5 7.0	15.0 10.5	1.5 1.5	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay E to Q _N	3.3 5.0	2.0 2.0	8.0 7.5	12.5 9.0	1.5 1.5	15.0 11.0	ns	3-6
t _{PLH}	Propagation Delay Address to Q _N	3.3 5.0	2.0 2.0	12.0 8.0	19.0 13.0	1.5 1.5	22.5 15.5	ns	3-6
t _{PHL}	Propagation Delay Address to Q _N	3.3 5.0	2.0 2.0	10.0 7.0	16.0 11.0	1.5 1.5	19.0 13.0	ns	3-6
t _{PHL}	Propagation Delay MR to Q	3.3 5.0	2.0 2.0	8.0 6.0	12.0 9.0	1.5 1.5	13.5 10.0	ns	3-7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to E	3.3 5.0		3.5 2.5	4.5 3.5	ns	3-9
t _h	Hold Time, HIGH or LOW D _n to E	3.3 5.0		2.5 2.0	2.5 2.0	ns	3-9
t _s	Setup Time Address to E	3.3 5.0		7.0 4.0	9.0 6.0	ns	3-6
t _h	Hold Time Address to E	3.3 5.0		2.0 2.0	2.0 2.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.0 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay Dn to Qn	5.0	2.0	6.5	11.0	1.5	12.5	ns	3-5
tPHL	Propagation Delay Dn to Qn	5.0	2.0	7.0	10.5	1.5	12.0	ns	3-5
tPLH	Propagation Delay E to Qn	5.0	2.0	10.5	14.0	1.5	16.5	ns	3-6
tPHL	Propagation Delay E to Qn	5.0	2.0	9.0	12.0	1.5	14.0	ns	3-6
tPLH	Propagation Delay Address to Qn	5.0	2.0	8.0	11.5	1.5	13.5	ns	3-6
tPHL	Propagation Delay Address to Qn	5.0	2.0	6.0	10.0	1.5	12.0	ns	3-6
tPLH	Propagation Delay MR to Q	5.0	2.0		10.0	1.5	11.0	ns	3-7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	VCC* (V)	74ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Dn to E	5.0		3.0	4.0	ns	3-9	
th	Hold Time, HIGH or LOW Dn to E	5.0		2.5	2.5	ns	3-9	
ts	Setup Time Address to E	5.0		4.5	6.5	ns	3-6	
th	Hold Time Address to E	5.0		2.5	2.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	50.0	pF	VCC = 5.0 V



MOTOROLA

MC74AC273 MC74ACT273

Octal D Flip-Flop

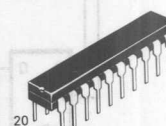
The MC74AC273/74ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

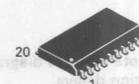
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- 'ACT273 Has TTL Compatible Inputs

OCTAL D FLIP-FLOP

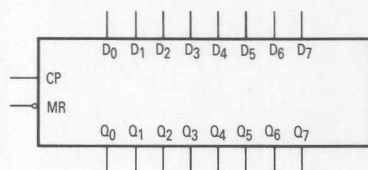


N SUFFIX
CASE 738-03
PLASTIC



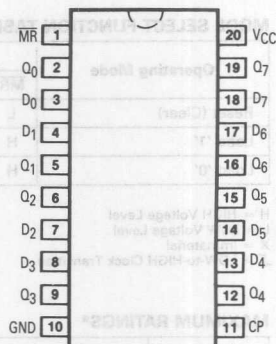
DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL



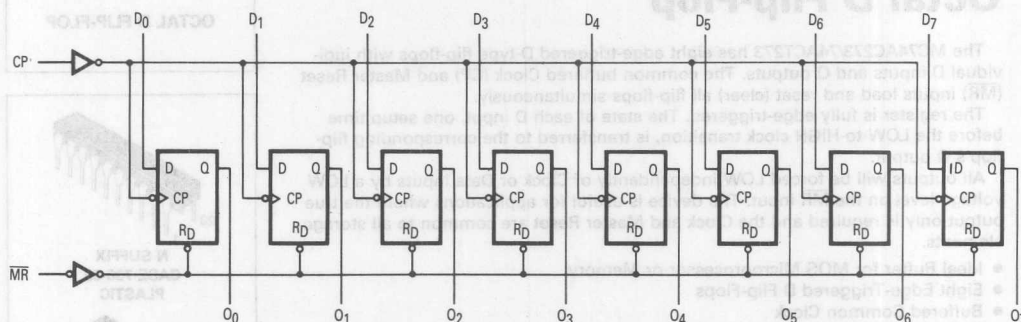
PIN NAMES

D₀–D₇ Data Inputs
MR Master Reset
CP Clock Pulse Input
Q₀–Q₇ Data Outputs



MC74AC273 • MC74ACT273

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	┐	H	H
Load '0'	H	┐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
┐ = LOW-to-HIGH Clock Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

FACT DATA

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 125		MHz	3-3
t _{PLH}	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.5	12.5 9.0	3.0 2.5	14.0 10.0	ns	3-6
t _{PHL}	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.5 11.0	ns	3-6
t _{PHL}	Propagation Delay MR to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.0 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW Data to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3-9	
t _h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	−2.0 −1.0	0 1.0	0 1.0	ns	3-9	
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3-6	
t _w	MR Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0	6.0 4.5	ns	3-6	
t _{rec}	Recovery Time MR to CP	3.3 5.0	1.5 1.0	3.5 2.0	4.5 3.0	ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	Units	Typ	Value
C _{IN}	Input Capacitance	pF	4.5	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	pF	50	V _{CC} = 5.0 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	125	200		125		MHz	3-3
t _{PLH}	Propagation Delay Clock to Output	5.0	3.0	6.0	10	2.5	11.0	ns	3-6
t _{PHL}	Propagation Delay Clock to Output	5.0	3.0	6.5	11	2.5	12.0	ns	3-6
t _{PHL}	Propagation Delay MR to Output	5.0	3.0	7.0	11	2.5	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW Data to CP	5.0	3.0	4.5	5.0	ns	3-9	
t _h	Hold Time, HIGH or LOW Data to CP	5.0	−2.5	2.0	2.0	ns	3-9	
t _w	Clock Pulse Width HIGH or LOW	5.0	2.5	4.0	4.5	ns	3-6	
t _w	MR Pulse Width HIGH or LOW	5.0	2.5	4.0	4.5	ns	3-6	
t _{rec}	Recovery Time MR to CP	5.0	−1.0	2.0	3.0	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	50	pF	VCC = 5.0 V

FACT DATA



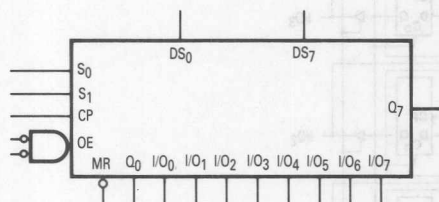
MOTOROLA

8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

The MC74AC299/74ACT299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 , Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT299 Has TTL Compatible Inputs

LOGIC SYMBOL

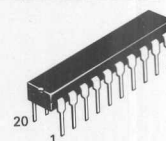


PIN NAMES

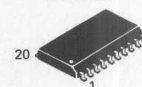
CP	Clock Pulse Input
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
S ₀ , S ₁	Mode Select Inputs
MR	Asynchronous Master Reset
OE ₁ , OE ₂	3-State Output Enable Inputs
I/O ₀ -I/O ₇	Parallel Data Inputs or 3-State Parallel Outputs
Q ₀ , Q ₇	Serial Outputs

**MC74AC299
MC74ACT299**

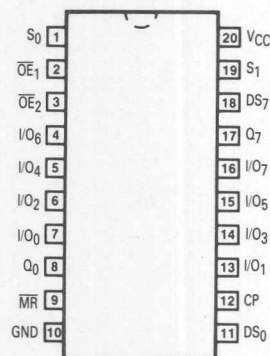
**8-INPUT UNIVERSAL
SHIFT/STORAGE
REGISTER WITH
COMMON
PARALLEL I/O PINS**



**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**

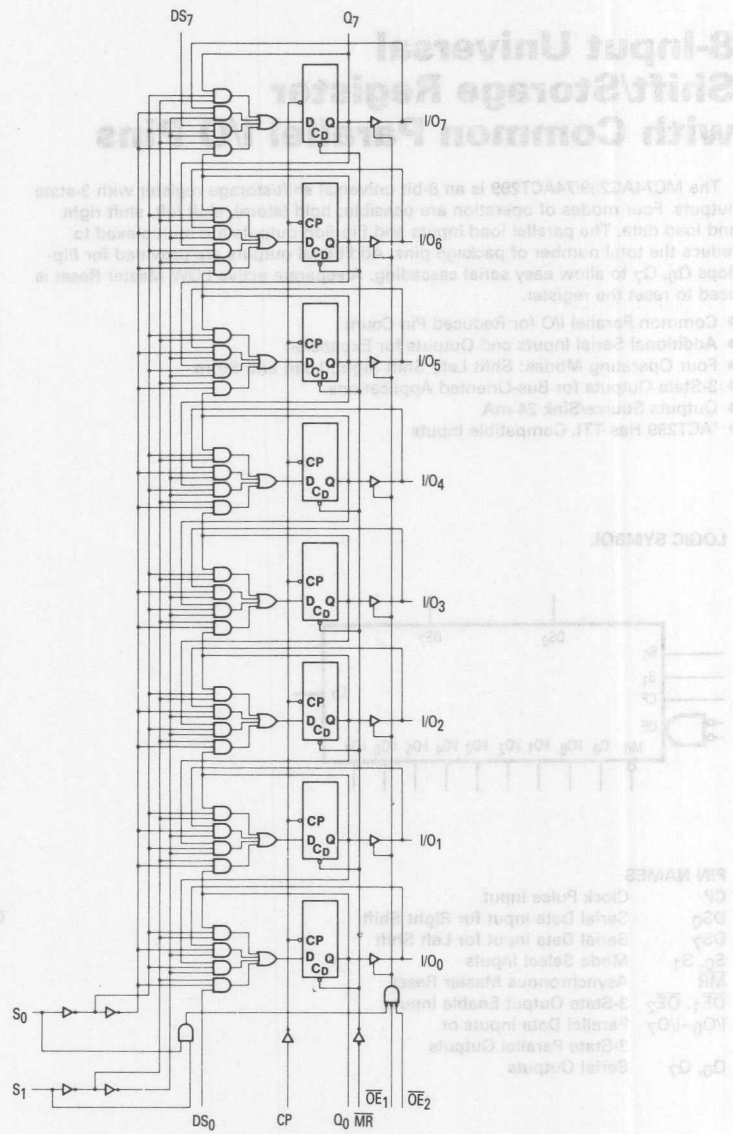
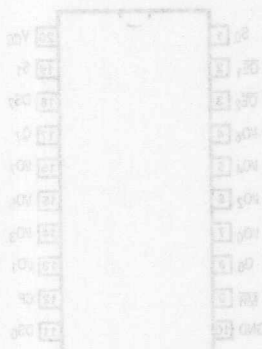


MC74AC299 • MC74ACT299



LOGIC DIAGRAM

8-INPUT UNIVERSAL
SHIFT-REGISTER WITH
COMMON
PARALLEL TO PINS



LOGIC SYMBOL

PIN NAMES
CP Clock Pulse Input
DS0 Serial Data Input for Left Shift
DS1 Serial Data Input for Right Shift
DS7 Mode Select Input
Q0 Asynchronous Master Reset
MR 3-State Output Enable Input
OE1 Parallel Data Input or 3-State Parallel Output
OE2 Serial Output

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

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FUNCTIONAL DESCRIPTION

The MC74AC299/74ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 , as shown in the Truth Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{MR} overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	150		ns/V
		$V_{CC} @ 4.5 V$	40		
		$V_{CC} @ 5.5 V$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	10		ns/V
		$V_{CC} @ 5.5 V$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

- V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

FACT DATA

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
V _{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I _{OUT} = -50 μA
		3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} = -24 mA -24 mA
V _{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I _{OUT} = 50 μA
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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Symbol	Parameter	Units	Typ	Max	Min
V _{CC}	Supply Voltage	V	5.0	5.5	3.0
V _{IH}	DC Input Voltage, Output Voltage (ref. to GND)	V	V _{CC}	0	0
t _{PLH}	†AC Devices except Schmitt inputs Input Rise and Fall Time (from 1)	ns	V _{CC} @ 3.0 V	150	100
			V _{CC} @ 4.5 V	40	30
			V _{CC} @ 5.5 V	25	15
			V _{CC} @ 3.0 V	10	5
t _{PLF}	†AC Devices except Schmitt inputs Input Rise and Fall Time (from 1)	ns	V _{CC} @ 3.0 V	150	100
			V _{CC} @ 4.5 V	40	30
			V _{CC} @ 5.5 V	25	15
			V _{CC} @ 3.0 V	10	5
T _J	Function Temperature (°C)	°C	140		
T _A	Operating Ambient Temperature Range	°C	25	-40	
I _{OH}	Output Current — High	mA	-24		
I _{OL}	Output Current — Low	mA	24		

1. V_{OH} from 50% to 100% V_{CC}; V_{OL} from 100% to 50% V_{CC}; rise/fall times for devices that differ from the typical input rise/fall times.
2. V_{OH} from 0.9 V to 3.0 V; V_{OL} from 3.0 V to 0.9 V; see individual data sheets for devices that differ from the typical input rise/fall times.

FACT DATA

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	3.3 5.0	90 130			80 105		MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	3.3 5.0	8.5 5.5		20.5 14	7.0 4.5	22 15	ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	3.3 5.0	8.5 5.5		21.5 14.5	7.0 5.0	23 16	ns	3-6
t _{PLH}	Propagation Delay CP to I/O _N	3.3 5.0	9.0 6.0		20.5 14.5	7.5 5.0	22.5 16	ns	3-6
t _{PHL}	Propagation Delay CP to I/O _N	3.3 5.0	10 6.5		23 16	8.5 6.0	24.5 17.5	ns	3-6
t _{PHL}	Propagation Delay MR to I/O _N	3.3 5.0	9.0 5.5		22.5 15.5	7.5 5.0	25.0 17.0	ns	3-6
t _{PHL}	Propagation Delay MR to I/O _N	3.3 5.0	9.0 5.5		21.5 15.0	7.5 5.0	24.0 16.5	ns	3-6
t _{PZH}	Output Enable Time OE to I/O _N	3.3 5.0	7.0 4.5		18 12.5	6.0 4.0	19.5 13.5	ns	3-7
t _{PZL}	Output Enable Time OE to I/O _N	3.3 5.0	7.0 5.0		18 12.5	6.0 4.0	20.5 14	ns	3-8
t _{PHZ}	Output Disable Time OE to I/O _N	3.3 5.0	6.5 3.5		18.5 14	5.5 3.0	19.5 15	ns	3-7
t _{PLZ}	Output Disable Time OE to I/O _N	3.3 5.0	5.5 3.5		17 12.5	4.5 2.0	19 13.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC299 • MC74ACT299

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0		8.5 5.0	8.5 5.5	ns	3-9	
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0		0.5 1.0	0.5 1.0	ns	3-9	
t _s	Setup Time, HIGH or LOW I/O _N to CP	3.3 5.0		5.5 3.5	6.0 4.0	ns	3-9	
t _h	Hold Time, HIGH or LOW I/O _N to CP	3.3 5.0		0 1.0	0 1.0	ns	3-9	
t _s	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	3.3 5.0		6.5 4.0	7.0 4.5	ns	3-6	
t _h	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	3.3 5.0		0 1.0	0.5 1.0	ns	3-6	
t _w	CP Pulse Width, LOW	3.3 5.0		4.5 3.5	5.0 3.5	ns	3-6	
t _w	MR Pulse Width, LOW	3.3 5.0		4.5 3.5	5.0 3.5	ns	3-9	
t _{rec}	Recovery Time MR to CP	3.3 5.0		1.5 1.5	1.5 1.5	ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	5.0	120			110		MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	5.0	4.0		12.5	3.0	14	ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	5.0	4.0		13.5	3.5	15	ns	3-6
t _{PLH}	Propagation Delay CP to I/O _N	5.0	4.5		12.5	4.5	13.5	ns	3-6
t _{PHL}	Propagation Delay CP to I/O _N	5.0	5.0		15	4.5	16.5	ns	3-6
t _{PLH}	Propagation Delay MR to Q ₀ or Q ₇	5.0	4.0		15	4.0	18	ns	3-6
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇	5.0	4.0		14.5	3.5	17.5	ns	3-6
t _{PZH}	Output Enable Time OE to I/O _N	5.0	2.5		12	1.5	13	ns	3-7
t _{PZL}	Output Enable Time OE to I/O _N	5.0	2.0		12	1.5	13.5	ns	3-8
t _{PHZ}	Output Disable Time OE to I/O _N	5.0	2.0		12.5	2.0	13.5	ns	3-7
t _{PLZ}	Output Disable Time OE to I/O _N	5.0	2.5		11.5	2.0	12.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC299 • MC74ACT299

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0		5.0	5.5	ns	3-9	
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0		1.0	1.0	ns	3-9	
t _s	Setup Time, HIGH or LOW I/O _n to CP	5.0		4.0	4.5	ns	3-9	
t _h	Hold Time, HIGH or LOW I/O _n to CP	5.0		1.0	1.0	ns	3-9	
t _s	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0		4.5	5.0	ns	3-6	
t _h	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0		1.0	1.0	ns	3-6	
t _w	CP Pulse Width HIGH or LOW	5.0		4.0	4.5	ns	3-9	
t _w	MR Pulse Width, LOW	5.0		3.5	3.5	ns	3-9	
t _{rec}	Recovery Time MR to CP	5.0		1.5	1.5	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	170	pF	V _{CC} = 5.0 V



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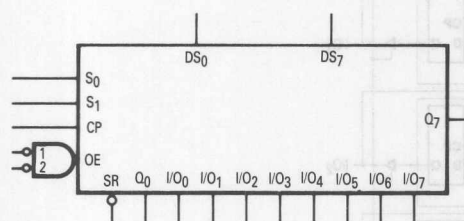
Product Preview

8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

The MC74AC323/74ACT323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the MC74AC299/74ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT323 Has TTL Compatible Inputs

LOGIC SYMBOL

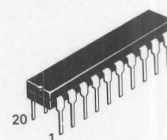


PIN NAMES

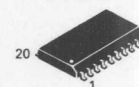
CP	Clock Pulse Input
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
S ₀ , S ₁	Mode Select Inputs
SR	Synchronous Master Reset
\overline{OE}_1 , \overline{OE}_2	3-State Output Enable Inputs
I/O ₀ -I/O ₇	Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs
Q ₀ , Q ₇	Serial Outputs

MC74AC323
MC74ACT323

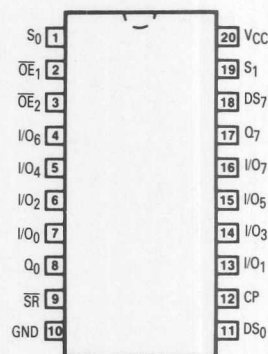
8-INPUT UNIVERSAL
SHIFT/STORAGE
REGISTER WITH
SYNCHRONOUS RESET
AND COMMON
I/O PINS



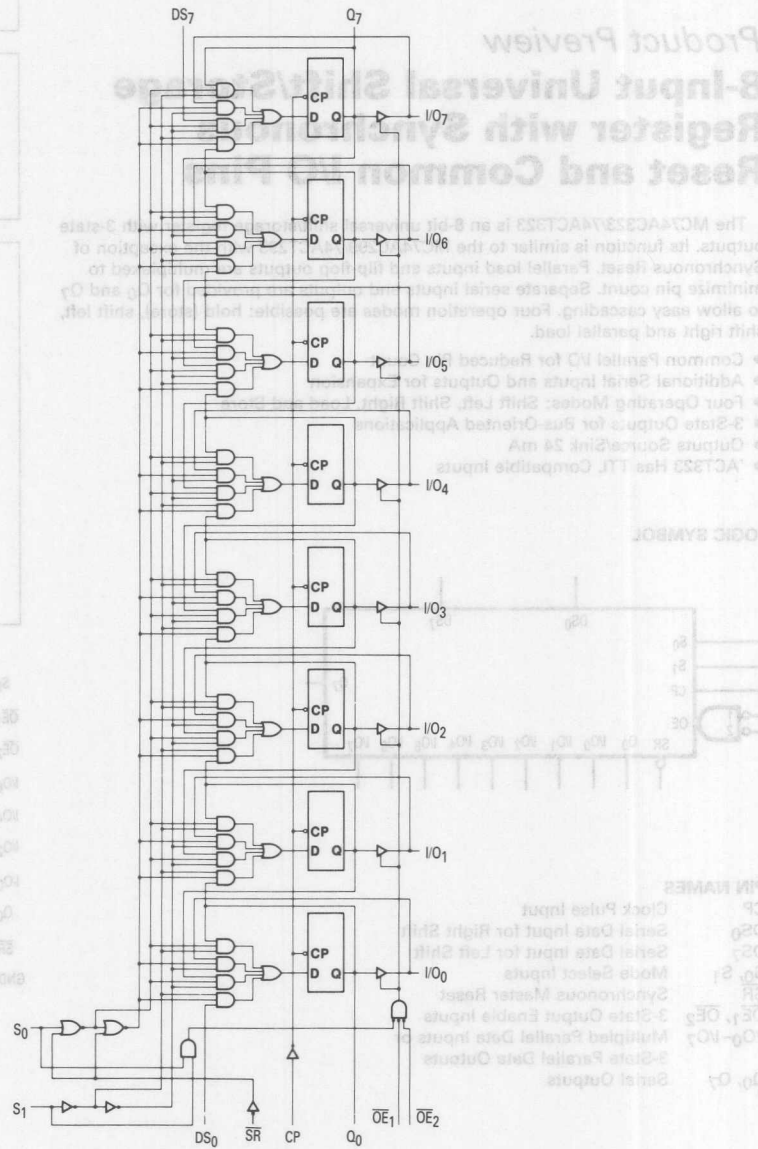
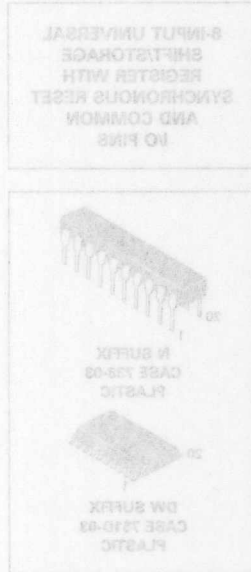
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FACT DATA

MC74AC323 • MC74ACT323

FUNCTIONAL DESCRIPTION

The MC74AC323/74ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{SR} overrides the Select inputs and allows the flip-flops to be reset by the next rising edge

of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

TRUTH TABLE

Inputs				Response
\overline{SR}	S_1	S_0	CP	
L	X	X	\downarrow	Synchronous Reset; Q_0 – Q_7 = LOW
H	H	H	\downarrow	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	\downarrow	Shift Right; $DS_0 \rightarrow Q_0, Q_0 \rightarrow Q_1$, etc.
H	H	L	\downarrow	Shift Left; $DS_7 \rightarrow Q_7, Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

\downarrow = LOW-to-HIGH Clock Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

I_{in}	Maximum Input Leakage Current	8.5	μA
I_{out}	Maximum Output Current	50	mA
I_{CC}	Maximum Quiescent Supply Current	2.5	mA

FACT DATA

MC74AC323 • MC74ACT323

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC323 • MC74ACT323

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} − 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	3.3 5.0		55 130				MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	3.3 5.0		31 12				ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	3.3 5.0		30 13				ns	3-6
t _{PLH}	Propagation Delay CP to I/O _n	3.3 5.0		28 11				ns	3-6
t _{PHL}	Propagation Delay CP to I/O _n	3.3 5.0		28 12				ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0		24 10				ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0		24 10				ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0		25 13				ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0		24 12				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC323 • MC74ACT323

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0	12 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0	0 0				ns	3-9
t _s	Setup Time, HIGH or LOW I/O _N , DS ₀ , DS ₇ to CP	3.3 5.0	5.0 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW I/O _N , DS ₀ , DS ₇ to CP	3.3 5.0	0 0				ns	3-9
t _s	Setup Time, HIGH or LOW SR to CP	3.3 5.0	4.0 2.0				ns	3-9
t _h	Hold Time, HIGH or LOW SR to CP	3.3 5.0	0 0				ns	3-9
t _w	CP Pulse Width HIGH or LOW	3.3 5.0	9.0 4.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	5.0	120	125		110		MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	5.0	5.0	9.0	12.5	4.0	14	ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	5.0	5.0	9.0	13.5	4.5	15	ns	3-6
t _{PLH}	Propagation Delay CP to I/O _N	5.0	5.0	8.5	12.5	4.5	14.5	ns	3-6
t _{PHL}	Propagation Delay CP to I/O _N	5.0	6.0	10	14.5	5.0	16	ns	3-6
t _{PZH}	Output Enable Time	5.0	3.5	7.5	11	3.0	12.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	3.0	13	ns	3-8
t _{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	3.0	13.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	2.5	12.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC323 • MC74ACT323



AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	5.0	ns	3-9	
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	0	1.5	1.5	ns	3-9	
t _s	Setup Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	1.0	4.0	4.5	ns	3-9	
t _h	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	0	1.0	1.0	ns	3-9	
t _s	Setup Time, HIGH or LOW SR to CP	5.0	1.0	2.5	2.5	ns	3-9	
t _h	Hold Time, HIGH or LOW SR to CP	5.0	0	1.0	1.0	ns	3-9	
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	170	pF	VCC = 5.0 V

FACT DATA



MOTOROLA

**MC74AC350
MC74ACT350**

Product Preview

4-Bit Shifter With 3-State Outputs

**4-BIT SHIFTER
WITH 3-STATE
OUTPUTS**

The MC74AC350/74ACT350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable (\overline{OE}) inputs as a third Select level. With appropriate interconnections, the 'AC/ACT350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

- Linking Inputs for Word Expansion
- 3-State Outputs for Extending Shift Range

FUNCTIONAL DESCRIPTION

The MC74AC350/74ACT350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1 . Outputs O_0 – O_3 are 3-state, controlled by an active-LOW output enable (\overline{OE}). When \overline{OE} is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC EQUATIONS

$$O_0 = \overline{S_0} \overline{S_1} I_0 + S_0 \overline{S_1} I_{-1} + \overline{S_0} S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$O_1 = \overline{S_0} \overline{S_1} I_1 + S_0 \overline{S_1} I_0 + \overline{S_0} S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$O_2 = \overline{S_0} \overline{S_1} I_2 + S_0 \overline{S_1} I_1 + \overline{S_0} S_1 I_0 + S_0 S_1 I_{-1}$$

$$O_3 = \overline{S_0} \overline{S_1} I_3 + S_0 \overline{S_1} I_2 + \overline{S_0} S_1 I_1 + S_0 S_1 I_0$$

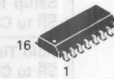
TRUTH TABLE

Inputs			Outputs			
\overline{OE}	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

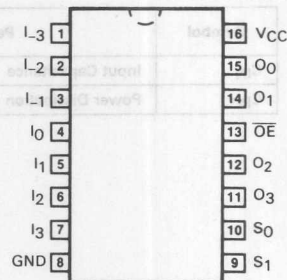
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**

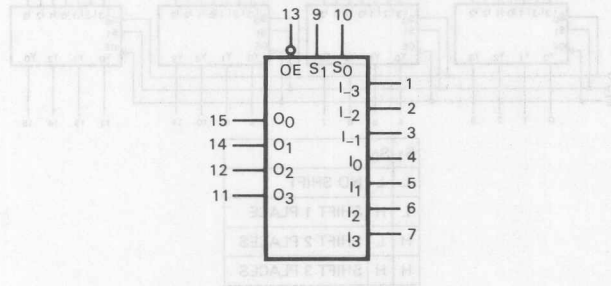


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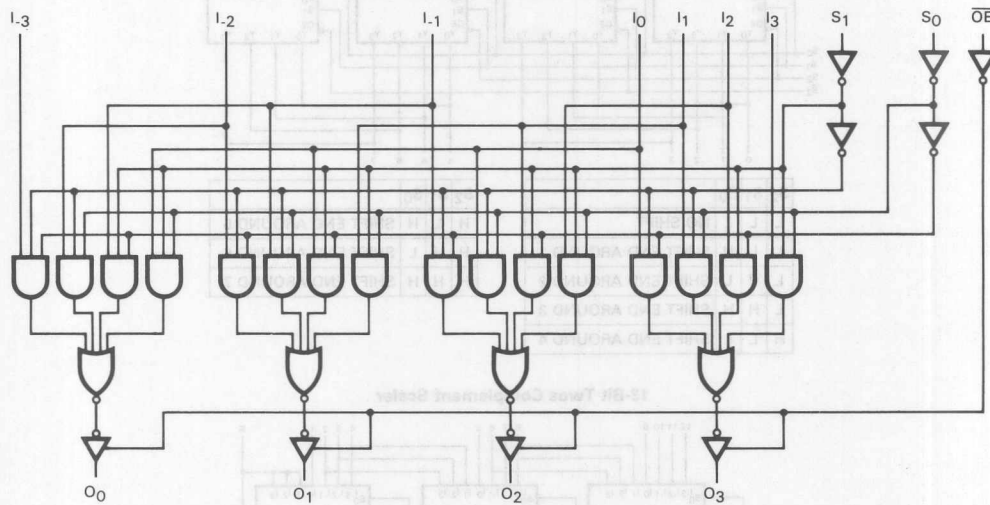
FACT DATA

MC74AC350 • MC74ACT350

LOGIC SYMBOL



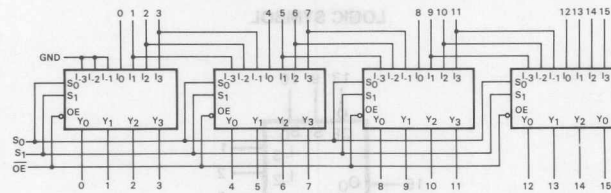
LOGIC DIAGRAM



MC74AC350 • MC74ACT350

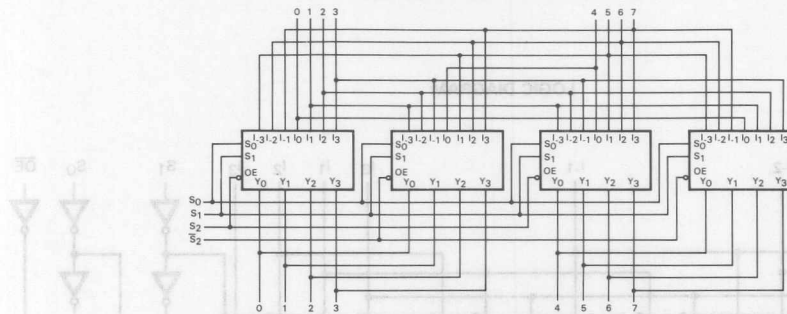
APPLICATIONS

16-Bit Shift-Up 0 to 3 Places, Zero Backfill



S ₁	S ₀	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

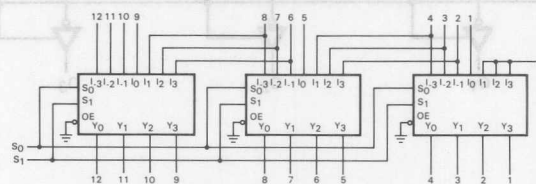
8-Bit End Around Shift 0 to 7 Places



S ₂	S ₁	S ₀	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4

S ₂	S ₁	S ₀	
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-Bit Twos Complement Scaler



S ₁	S ₀	SCALE
L	$L \div 8$	1/8
L	$H \div 4$	1/4
H	$L \div 2$	1/2
H	H NO CHANGE	1

MC74AC350 • MC74ACT350

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC 2.0	5.0	6.0	V
		'ACT 4.5	5.0	5.5	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V 150	40		ns/V
		V _{CC} @ 4.5 V	25		
		V _{CC} @ 5.5 V			
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V 10	8.0		ns/V
		V _{CC} @ 5.5 V			
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

I _{CC}	Supply Current	50	50	50	mA
I _{OH}	Output Current — High	24	24	24	mA
I _{OL}	Output Current — Low	24	24	24	mA

*All ratings are based on a single unit tested at 25°C. Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC350 • MC74ACT350

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
V _{OL}	Maximum Low Level Output Voltage	3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
V _{OL}	Maximum Low Level Output Voltage	3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC350 • MC74ACT350

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay I _n to O _n	3.3 5.0						ns	3-5
t _{PHL}	Propagation Delay I _n to O _n	3.3 5.0						ns	3-5
t _{PLH}	Propagation Delay S _n to O _n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay S _n to O _n	3.3 5.0						ns	3-6
t _{PZH}	Output Enable to O _n	3.3 5.0						ns	3-7
t _{PZL}	Output Enable to O _n	3.3 5.0						ns	3-8
t _{PHZ}	Output Enable to O _n	3.3 5.0						ns	3-7
t _{PLZ}	Output Enable to O _n	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC350 • MC74ACT350

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay I _N to O _N	5.0						ns	3-6
t _{PHL}	Propagation Delay I _N to O _N	5.0						ns	3-6
t _{PLH}	Propagation Delay S _N to O _N	5.0						ns	3-6
t _{PHL}	Propagation Delay S _N to O _N	5.0						ns	3-6
t _{PZH}	Output Enable to O _N	5.0						ns	3-7
t _{PZL}	Output Enable to O _N	5.0						ns	3-8
t _{PHZ}	Output Enable to O _N	5.0						ns	3-7
t _{PLZ}	Output Enable to O _N	5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
CPD	Power Dissipation Capacitance	40.0	pF	V _{CC} = 5.0 V

Symbol	Parameter	VCC* (V)	74AC			Units	Fig.
			TA = +25°C CL = 50 pF				
			Min	Typ	Max		
tPLH	Propagation Delay In to On	3.3 5.0				ns	3-6
tPHL	Propagation Delay In to On	3.3 5.0				ns	3-6
tPLH	Propagation Delay Sn to On	3.3 5.0				ns	3-6
tPHL	Propagation Delay Sn to On	3.3 5.0				ns	3-6
tPZH	Output Enable to On	3.3 5.0				ns	3-7
tPZL	Output Enable to On	3.3 5.0				ns	3-8
tPHZ	Output Enable to On	3.3 5.0				ns	3-7
tPLZ	Output Enable to On	3.3 5.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V
*Voltage Range 2.3 is 2.3 V ± 0.3 V
*Voltage Range 0.0 is 0.0 V ± 0.5 V

FACT DATA



MOTOROLA

MC74AC352 MC74ACT352

Dual 4-Input Multiplexer

The MC74AC352/74ACT352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The MC74AC352/74ACT352 is the functional equivalent of the MC74AC353/74ACT353 except with inverted outputs.

- Inverted Version of the MC74AC353/74ACT353
- Separate Enables for Each Multiplexer
- Outputs Source/Sink 24 mA
- 'ACT352 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

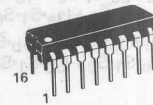
- I_{0a}–I_{3a} Side A Data Inputs
- I_{0b}–I_{3b} Side B Data Inputs
- S₀, S₁ Common Select Inputs
- E_a Side A Enable Input
- E_b Side B Enable Input
- Z_a, Z_b Multiplexer Outputs

TRUTH TABLE

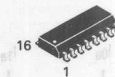
Select Inputs		\bar{E}	Inputs (a or b)				Outputs
S ₀	S ₁		I ₀	I ₁	I ₂	I ₃	\bar{Z}
X	X	H	X	X	X	X	H
L	L	L	X	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

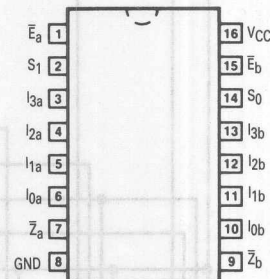
DUAL 4-INPUT MULTIPLEXER



N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC



MC74AC352 • MC74ACT352

FUNCTIONAL DESCRIPTION

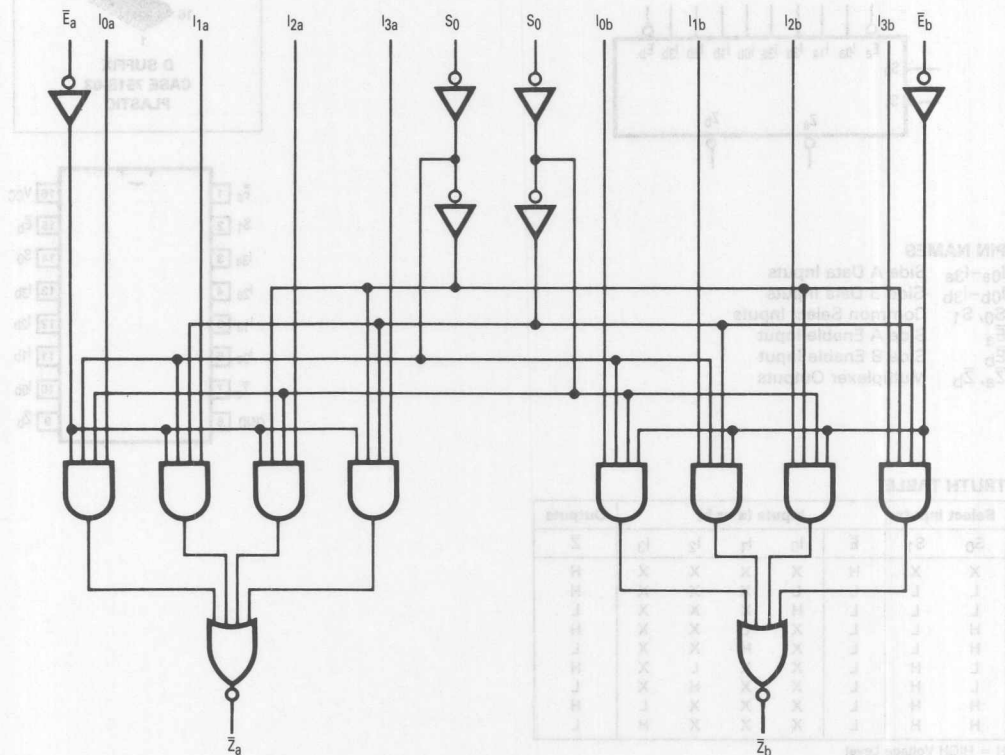
The MC74AC352/74ACT352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a, \bar{E}_b) which can be used to strobe the outputs independently. When the Enables (\bar{E}_a, \bar{E}_b) are HIGH, the corresponding outputs (\bar{Z}_a, \bar{Z}_b) are forced HIGH.

The logic equations for the outputs are shown below:

$$\begin{aligned}\bar{Z}_a &= \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + \\ &\quad I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0) \\ \bar{Z}_b &= \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + \\ &\quad I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)\end{aligned}$$

The MC74AC352/74ACT352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The MC74AC352/74ACT352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

MC74AC352 • MC74ACT352

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to $V_{CC}+0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to $V_{CC}+0.5$	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	150		ns/V
		V_{CC} @ 4.5 V	40		
		V_{CC} @ 5.5 V	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	10		ns/V
		V_{CC} @ 5.5 V	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	−40	25	85	°C
I_{OH}	Output Current — High			−24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC352 • MC74ACT352

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC352 • MC74ACT352

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	3.3 5.0	2.0 2.0	8.5 6.5	15.0 11.0	1.0 1.0	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay S _n to Z _n	3.3 5.0	2.0 2.0	8.0 6.0	14.5 11.0	1.0 1.0	16.5 12.0	ns	3-6
t _{PLH}	Propagation Delay E _n to Z _n	3.3 5.0	2.0 2.0	6.0 4.5	13.5 9.5	1.0 1.0	16.0 11.0	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	3.3 5.0	2.0 2.0	5.5 4.0	11.0 8.0	1.0 1.0	12.5 9.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	2.0 2.0	7.0 5.0	12.5 9.0	1.0 1.0	14.5 10.5	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	2.0 2.0	7.0 5.0	11.5 8.5	1.0 1.0	13.0 10.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	5.0	3.0	6.0	9.0	1.0	9.5	ns	3-6
t _{PHL}	Propagation Delay S _n to Z _n	5.0	3.0	6.0	9.0	1.0	9.5	ns	3-6
t _{PLH}	Propagation Delay E _n to Z _n	5.0	2.0	4.5	8.0	1.0	8.5	ns	3-6
t _{PHL}	Propagation Delay E _n to Z _n	5.0	2.0	4.5	8.0	1.0	8.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	2.0	5.5	8.5	1.0	9.0	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	5.0	2.0	6.5	8.5	1.0	9.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V



MOTOROLA

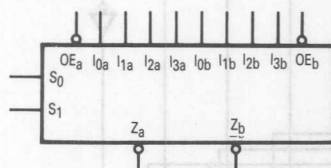
**MC74AC353
MC74ACT353**

Dual 4-Input Multiplexer with 3-State Outputs

The MC74AC353/74ACT353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (\overline{OE}) inputs, allowing the outputs to interface directly with bus-oriented systems.

- Inverted Version of the MC74AC253/74ACT253
- Multifunction Capability
- Separate Enables for Each Multiplexer
- Outputs Source/Sink 24 mA
- 'ACT353 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

I0a-I3a Side A Data Inputs
I0b-I3b Side B Data Inputs
S0, S1 Common Select Inputs
 \overline{OE}_a Side A Enable Input
 \overline{OE}_b Side B Enable Input
 $\overline{Z}_a, \overline{Z}_b$ Multiplexer Outputs

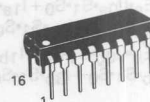
TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Outputs
S0	S1	I0	I1	I2	I3	\overline{OE}	\overline{Z}
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	L	H	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

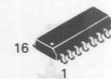
Address inputs S0 and S1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

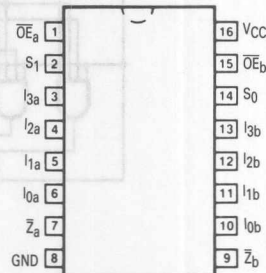
**DUAL 4-INPUT
MULTIPLEXER
WITH 3-STATE OUTPUTS**



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**



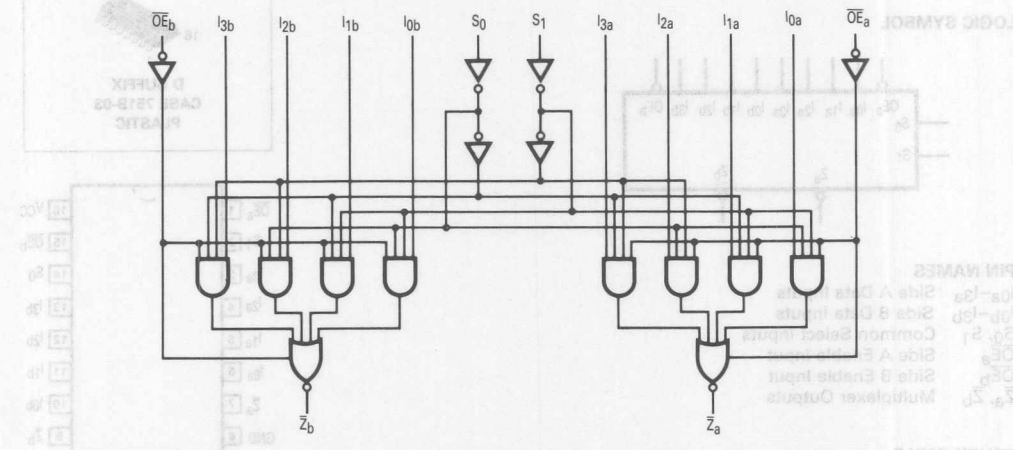
FUNCTIONAL DESCRIPTION

The MC74AC353/74ACT353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a, \overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	- 65 to + 150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC353 • MC74ACT353

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GD} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC353 • MC74ACT353

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	3.3 5.0	3.0 3.0		15.5 11.0	2.0 2.0	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay S _n to Z _n	3.3 5.0	3.0 3.0		16.0 11.5	2.0 2.0	18.0 13.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	2.0 2.0		14.5 10.0	1.0 1.0	17.0 11.5	ns	3-6
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	2.0 2.0		13.0 9.5	1.0 1.0	15.0 11.0	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	1.0 1.0		8.0 6.0	0.5 0.5	8.5 6.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.0 1.0		8.0 6.0	0.5 0.5	9.0 7.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	2.0 2.0		9.5 8.0	1.0 1.0	10.0 8.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 2.0		8.0 6.0	1.0 1.0	9.0 7.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC353 • MC74ACT353



AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	5.0	3.0		8.5	2.5	9.0	ns	3-6
t _{PHL}	Propagation Delay S _n to Z _n	5.0	3.0		8.5	2.5	9.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	2.0		8.0	1.5	8.5	ns	3-6
t _{PHL}	Propagation Delay I _n to Z _n	5.0	2.0		8.0	1.5	9.0	ns	3-6
t _{PZH}	Output Enable Time	5.0	1.0		7.0	1.0	7.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.0		7.5	1.0	8.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.0		9.0	1.0	10	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.0		7.0	1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
CPD	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V



MOTOROLA

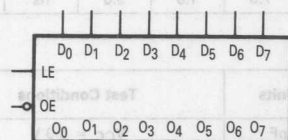
**MC74AC373
MC74ACT373**

Octal Transparent Latch with 3-State Outputs

The MC74AC373/74ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- ACT373 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

D₀-D₇ Data Inputs
LE Latch Enable Input
OE Output Enable Input
O₀-O₇ 3-State Latch Outputs

TRUTH TABLE

Inputs			Outputs
OE	LE	D _n	O _n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O ₀

H = HIGH Voltage Level

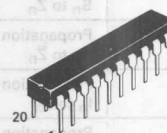
L = LOW Voltage Level

Z = High Impedance

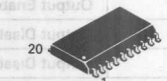
X = Immaterial

O₀ = Previous O₀ before LOW-to-HIGH Transition of Clock

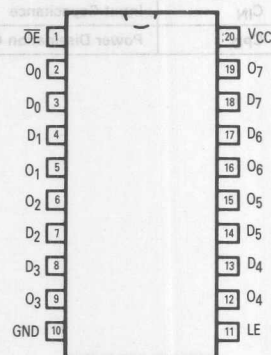
**OCTAL TRANSPARENT
LATCH WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**



FACT DATA

5-220

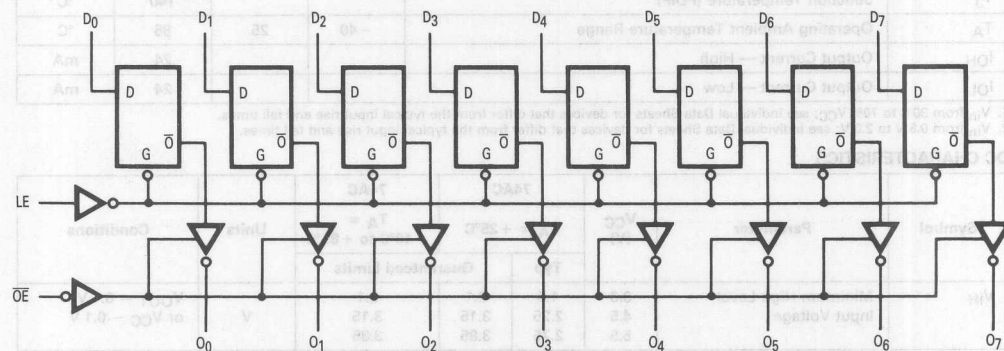
MC74AC373 • MC74ACT373

FUNCTIONAL DESCRIPTION

The MC74AC373/74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time

preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

FACT DATA

MC74AC373 • MC74ACT373

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC373 • MC74ACT373

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	10 7.0	13.5 9.5	1.5 1.5	15 10.5	ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	9.5 7.0	13 9.5	1.5 1.5	14.5 10.5	ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	10 7.5	13.5 9.5	1.5 1.5	15 10.5	ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	9.5 7.0	12.5 9.5	1.5 1.5	14 10.5	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	9.0 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	8.5 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	1.5 1.5	10 8.0	12.5 11	1.0 1.0	14.5 12.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC373 • MC74ACT373

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	3.3	3.5	5.5	6.0	ns	3-9	
		5.0	2.0	4.0	4.5			
t _h	Hold Time, HIGH or LOW D _n to LE	3.3	−3.0	1.0	1.0	ns	3-9	
		5.0	−1.5	1.0	1.0			
t _w	LE Pulse Width, HIGH	3.3	4.0	5.5	6.0	ns	3-6	
		5.0	2.0	4.0	4.5			

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.5	8.5	10	1.5	11.5	ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	5.0	2.0	8.0	10	1.5	11.5	ns	3-5
t _{PLH}	Propagation Delay LE to O _n	5.0	2.5	8.5	11	2.0	11.5	ns	3-6
t _{PHL}	Propagation Delay LE to O _n	5.0	2.0	8.0	10	1.5	11.5	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0	7.5	9.0	1.5	10.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	2.5	9.0	11	2.5	12.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5	7.5	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	3.0	7.0	8.0	ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	0	0	1.0	ns	3-9
t _w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	40	pF	VCC = 5.0 V

FACT DATA



MOTOROLA

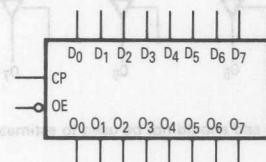
MC74AC374 MC74ACT374

Octal D-Type Flip-Flop with 3-State Outputs

The MC74AC374/74ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- See MC74AC273 for Reset Version
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC574 for Broadside Pinout Version
- See MC74AC564 for Broadside Pinout Version with Inverted Outputs
- 'ACT374 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

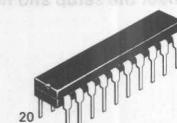
D₀-D₇ Data Inputs
CP Clock Pulse Input
 \overline{OE} 3-State Output Enable Input
Q₀-Q₇ 3-State Outputs

TRUTH TABLE

Inputs			Outputs
D _n	CP	\overline{OE}	O _n
H	┐	L	H
L	┐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
┐ = LOW-to-HIGH Transition

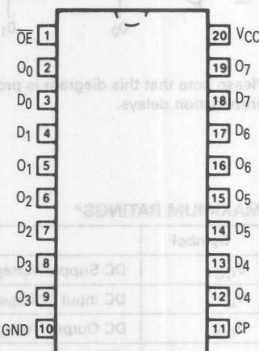
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS



N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

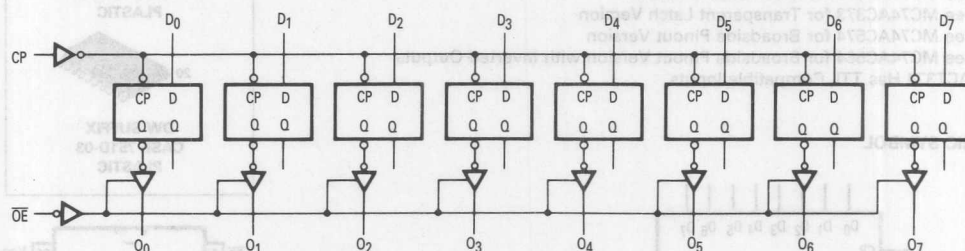


FUNCTIONAL DESCRIPTION

The MC74AC374/74ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the

LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

FACT DATA

MC74AC374 • MC74ACT374

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC374 • MC74ACT374

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
			4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = −24 mA −24 mA
			5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
			4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA 24 mA
			5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	60 100	110 155		60 100		MHz	3-3
t _{PLH}	Propagation Delay CP to O _N	3.3 5.0	3.0 2.5	11 8.0	13.5 9.5	1.5 1.5	15.5 10.5	ns	3-6
t _{PHL}	Propagation Delay CP to O _N	3.3 5.0	2.5 2.0	10 7.0	12.5 9.0	2.0 1.5	14 10	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 7.0	11.5 8.5	1.5 1.0	13 9.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 2.0	9.0 6.5	11.5 8.5	1.5 1.0	13 9.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	3.0 2.0	10.5 8.0	12.5 11	2.0 2.0	14.5 12.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC374 • MC74ACT374



AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3	2.0	5.5	6.0	ns	3-9	
		5.0	1.0	4.0	4.5			
t _h	Hold Time, HIGH or LOW D _n to CP	3.3	-1.0	1.0	1.0	ns	3-9	
		5.0	0	1.5	1.5			
t _w	CP Pulse Width HIGH or LOW	3.3	4.0	5.5	6.0	ns	3-6	
		5.0	2.5	4.0	4.5			

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	100	160		90		MHz	3-3
tPLH	Propagation Delay CP to ON	5.0	2.0	8.5	10	2.0	11.5	ns	3-6
tPHL	Propagation Delay CP to ON	5.0	2.0	8.0	9.5	1.5	11	ns	3-6
tPZH	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns	3-7
tPZL	Output Enable Time	5.0	1.5	8.0	9.0	1.5	10.5	ns	3-8
tPHZ	Output Disable Time	5.0	1.5	8.5	11.5	1.0	12.5	ns	3-7
tPLZ	Output Disable Time	5.0	1.5	7.0	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	1.0	7.0	8.0	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	0	1.5	1.5	ns	3-9	
t _w	CP Pulse Width HIGH or LOW	5.0	2.5	7.0	8.0	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	80	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

MC74AC377 MC74ACT377

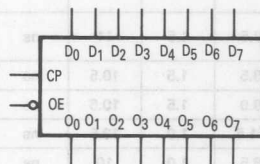
Octal D Flip-Flop with Clock Enable

The MC74AC377/74ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

- Ideal for Addressable Register Applications
- Clock Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Outputs Source/Sink 24 mA
- See MC74AC273 for Master Reset Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- 'ACT377 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

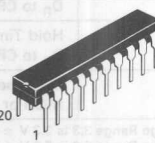
D₀–D₇ Data Inputs
CE Clock Enable (Active LOW)
Q₀–Q₇ Data Outputs
CP Clock Pulse Input

MODE SELECT-FUNCTION TABLE

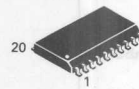
Operating Mode	Inputs			Outputs
	CP	CE	D _n	Q _n
Load '1'		L	H	H
Load '0'		L	L	L
Hold (Do Nothing)		H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

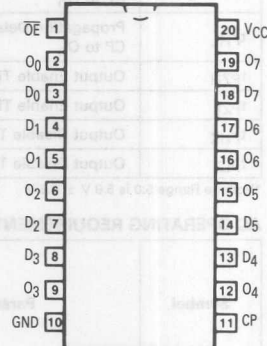
OCTAL D
FLIP-FLOP WITH
CLOCK ENABLE



N SUFFIX
CASE 738-03
PLASTIC

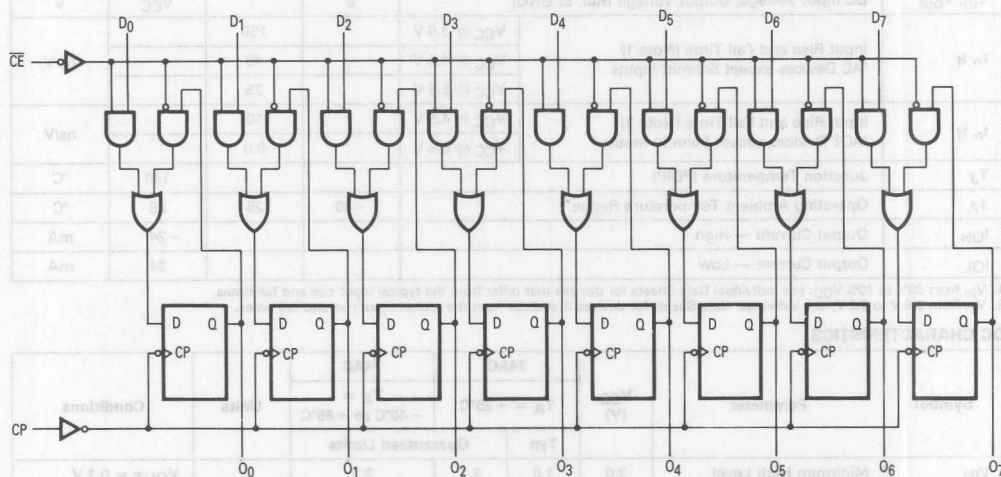


DW SUFFIX
CASE 751D-03
PLASTIC



MC74AC377 • MC74ACT377

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC377 • MC74ACT377

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = - 50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} = - 24 mA - 24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			- 75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC377 • MC74ACT377

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140			75 125		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _N	3.3 5.0	3.0 2.0		13 9.0	1.5 1.5	14 10	ns	3-6
t _{PHL}	Propagation Delay CP to Q _N	3.3 5.0	3.5 2.5		13 10	2.0 1.5	14.5 11	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	Units	Test Conditions
C _{IN}	Input Capacitance	pF	V _{CC} = 5.0 V
C _P	Power Dissipation Capacitance	pF	V _{CC} = 5.0 V

FACT DATA

MC74AC377 • MC74ACT377

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3		5.5	6.0	ns	3-9	
		5.0		4.0	4.5			
t _h	Hold Time, HIGH or LOW D _n to CP	3.3		0	0	ns	3-9	
		5.0		1.0	1.0			
t _s	Setup Time, HIGH or LOW CE to CP	3.3		6.0	7.5	ns	3-9	
		5.0		4.0	4.5			
t _h	Hold Time, HIGH or LOW CE to CP	3.3		0	0	ns	3-9	
		5.0		1.0	1.0			
t _w	CP Pulse Width HIGH or LOW	3.3		5.5	6.0	ns	3-6	
		5.0		4.0	4.5			

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	140			125		MHz	3-3
tPLH	Propagation Delay CP to Qn	5.0	3.0		9.0	2.5	10	ns	3-6
tPHL	Propagation Delay CP to Qn	5.0	2.5		10	2.5	11	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	VCC* (V)	74ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Dn to CP	5.0		4.5	5.5	ns	3-9	
th	Hold Time, HIGH or LOW Dn to CP	5.0		1.0	1.0	ns	3-9	
ts	Setup Time, HIGH or LOW CE to CP	5.0		4.5	5.5	ns	3-9	
th	Hold Time, HIGH or LOW CE to CP	5.0		1.0	1.0	ns	3-9	
tw	CP Pulse Width HIGH or LOW	5.0		4.0	4.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	90	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

MC74AC378 MC74ACT378

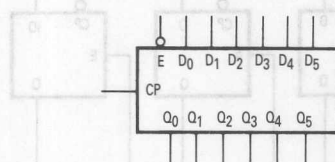
**PARALLEL
D REGISTER
WITH ENABLE**

Parallel D Register with Enable

The MC74AC378/74ACT378 is a 6-bit register with a buffered common Enable. This device is similar to the MC74AC174/74ACT174, but with common Enable rather than common Master Reset.

- 6-Bit High-Speed Parallel Register
- Positive Edge-Triggered D-Type Inputs
- Fully Buffered Common Clock and Enable Inputs
- Outputs Source/Sink 24 mA
- 'ACT378 Has TTL Compatible Inputs

LOGIC SYMBOL



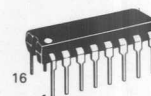
PIN NAMES

E Enable Input
D₀-D₅ Data Inputs
CP Clock Pulse Input
Q₀-Q₅ Outputs

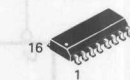
TRUTH TABLE

Inputs			Outputs
\bar{E}	CP	D _n	Q _n
H	⌋	X	No Change
L	⌋	H	H
L	⌋	L	L

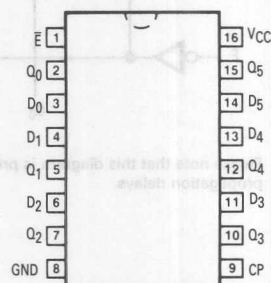
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌋ = LOW-to-HIGH Transition



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**



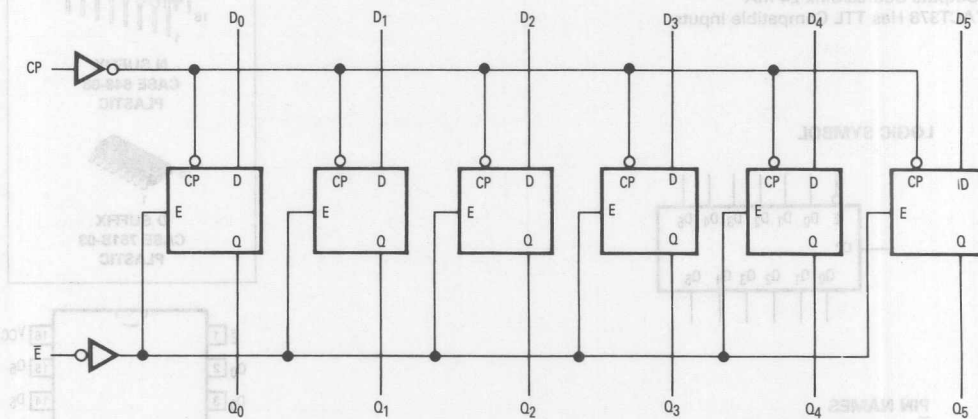
MC74AC378 • MC74ACT378

FUNCTIONAL DESCRIPTION

The MC74AC378/74ACT378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops.

When the \bar{E} input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the \bar{E} input is HIGH, the register will retain the present data independent of the CP input.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC378 • MC74ACT378

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	125 160			110 145		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	2.5 1.5		11 8.0	2.5 1.5	12.5 9.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	2.5 1.5		10.5 7.5	2.5 1.5	11 8.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC378 • MC74ACT378

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0		3.0 2.0	3.5 2.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0		2.0 2.0	2.0 2.0	ns	3-9	
t _s	Setup Time, HIGH or LOW E to CP	3.3 5.0		2.0 2.0	2.0 2.0	ns	3-9	
t _h	Hold Time, HIGH or LOW E to CP	3.3 5.0		2.0 2.0	2.0 2.0	ns	3-9	
t _w	CP Pulse Width HIGH or LOW	3.3 5.0		4.5 3.5	5.5 4.0	ns	3-6	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	140			120		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n	5.0	2.0		10	1.5	11	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n	5.0	2.0		11	1.5	12	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _N to CP	5.0	-0.5	1.0	1.0	ns	3-9
t _h	Hold Time, HIGH or LOW D _N to CP	5.0	1.0	1.5	1.5	ns	3-9
t _s	Setup Time, HIGH or LOW E to CP	5.0	-0.5	1.0	1.0	ns	3-9
t _h	Hold Time, HIGH or LOW E to CP	5.0	2.5	3.5	4.0	ns	3-9
t _w	CP Pulse Width HIGH or LOW	5.0		3.0	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	28	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

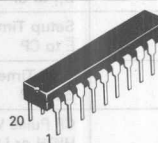
MC74AC521 MC74ACT521

8-Bit Identity Comparator

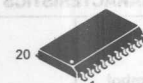
The MC74AC521/74ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\bar{I}_A = B$ also serves as an active LOW enable input.

- Compares Two 8-Bit Words in 6.5 ns Typ
- Expandable to Any Word Length
- 20-Pin Package
- Outputs Source/Sink 24 mA
- 'ACT521 has TTL-Compatible Inputs

8-BIT IDENTITY COMPARATOR

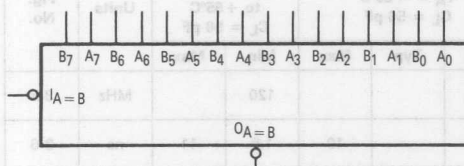


N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL



PIN NAMES

- A₀-A₇ Word A Inputs
B₀-B₇ Word B Inputs
 $\bar{I}_A = B$ Expansion or Enable Input
 $\bar{O}_A = B$ Identity Output

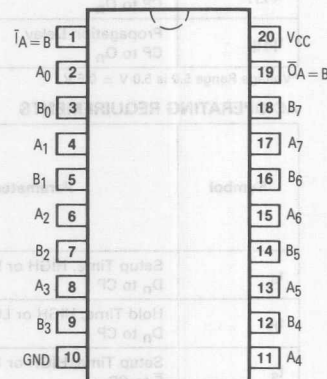
TRUTH TABLE

Inputs		Outputs
$\bar{I}_A = B$	A, B	$\bar{O}_A = B$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level

L = LOW Voltage Level

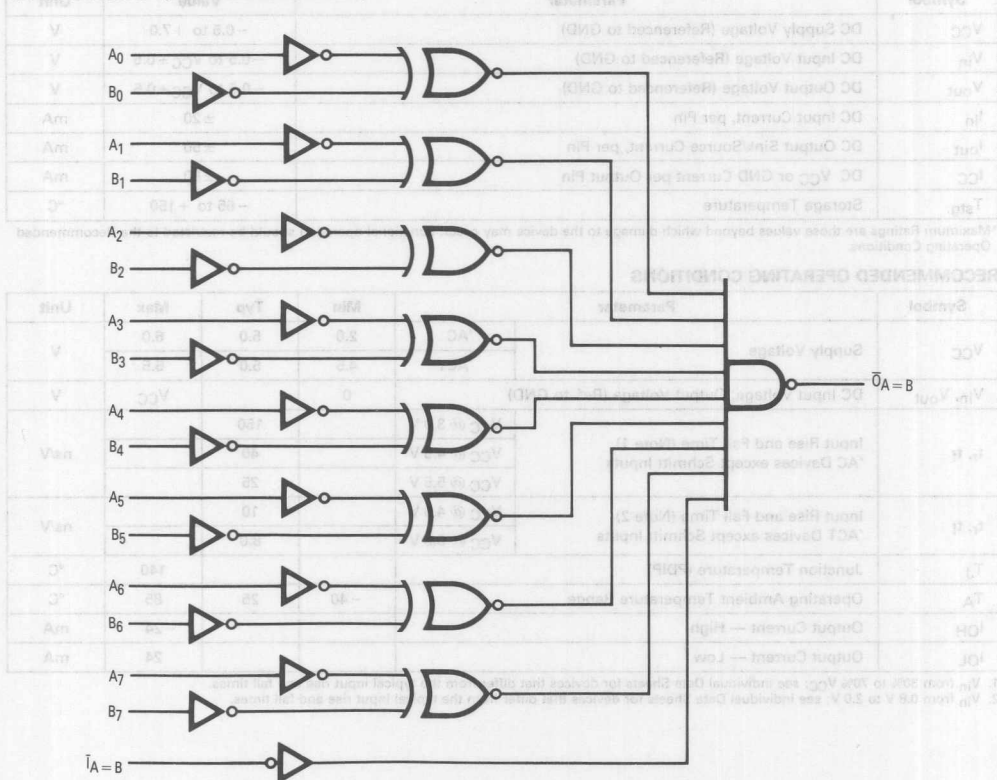
*A₀ = B₀, A₁ = B₁, A₂ = B₂, etc.



FACT DATA

MC74AC521 • MC74ACT521

LOGIC DIAGRAM (MC74AC521/74ACT521)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC521 • MC74ACT521

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0\text{ V}$	150		ns/V
		$V_{CC} @ 4.5\text{ V}$	40		
		$V_{CC} @ 5.5\text{ V}$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5\text{ V}$	10		ns/V
		$V_{CC} @ 5.5\text{ V}$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	−40	25	85	°C
I_{OH}	Output Current — High			−24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC521 • MC74ACT521

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC521 • MC74ACT521

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA –24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC521 • MC74ACT521

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n or B _n to $\bar{O}_A=B$	3.3 5.0	3.5 2.5		11 8.0	3.0 2.0	12 9.0	ns	3-6
t _{PHL}	Propagation Delay A _n or B _n to $\bar{O}_A=B$	3.3 5.0	4.5 3.0		11.5 8.5	3.5 2.5	12.5 9.0	ns	3-6
t _{PLH}	Propagation Delay $\bar{I}_A=B$ to $\bar{O}_A=B$	3.3 5.0	3.0 2.5		8.0 6.0	2.5 2.0	9.0 7.0	ns	3-6
t _{PHL}	Propagation Delay $\bar{I}_A=B$ to $\bar{O}_A=B$	3.3 5.0	3.0 2.0		8.0 6.0	2.5 2.0	9.0 7.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

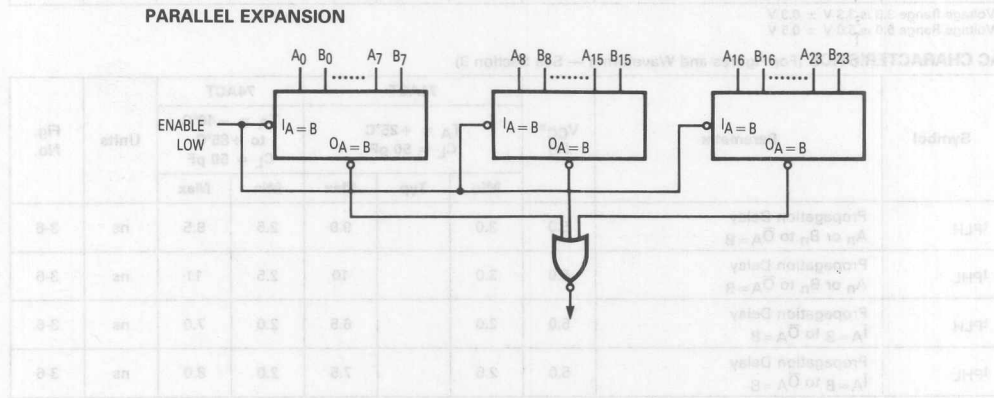
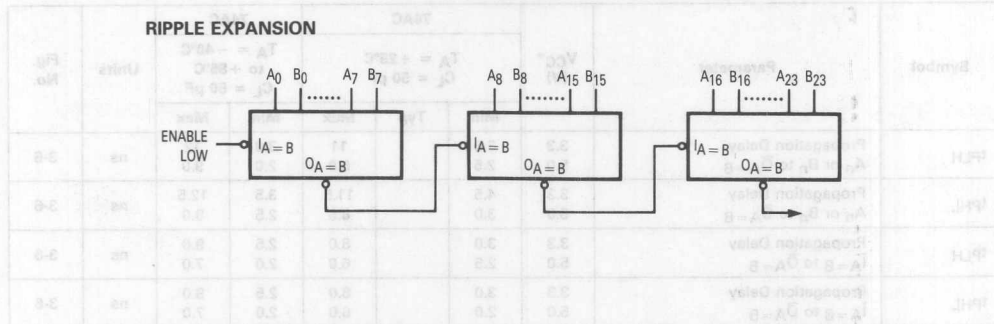
Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n or B _n to $\bar{O}_A = B$	5.0	3.0		9.0	2.5	9.5	ns	3-6
t _{PHL}	Propagation Delay A _n or B _n to $\bar{O}_A = B$	5.0	3.0		10	2.5	11	ns	3-6
t _{PLH}	Propagation Delay $\bar{I}_A = B$ to $\bar{O}_A = B$	5.0	2.0		6.5	2.0	7.0	ns	3-6
t _{PHL}	Propagation Delay $\bar{I}_A = B$ to $\bar{O}_A = B$	5.0	2.5		7.5	2.0	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V

APPLICATIONS



Symbol	Parameter	Unit	Test Conditions
C_{in}	Input Capacitance	pF	$V_{CC} = 5.0\text{ V}$
C_{PD}	Power Dissipation Capacitance	nF	$V_{CC} = 5.0\text{ V}$



MOTOROLA

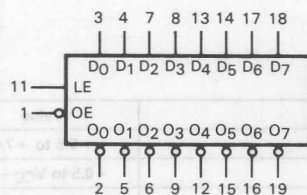
Product Preview

Octal Transparent Latch with 3-State Outputs

The MC74AC533/74ACT533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state. The 'AC/ACT533 is the same as the 'AC/ACT373, except that the outputs are inverted. For description and logic diagram please see the 'AC/ACT373 data sheet.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- 'ACT533 Has TTL Compatible Inputs
- Inverted Output Version of 'ACT373

LOGIC SYMBOL



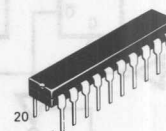
VCC = Pin 20
GND = Pin 10

PIN NAMES

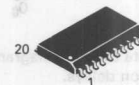
D₀-D₇ Data Inputs
LE Latch Enable Input
 \overline{OE} Output Enable Input
O₀-O₇ Complementary 3-State Outputs

**MC74AC533
MC74ACT533**

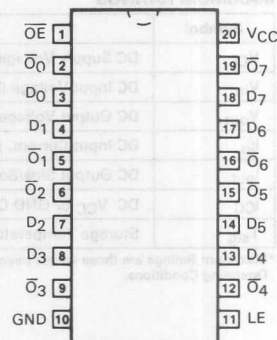
**OCTAL TRANSPARENT
LATCH WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**

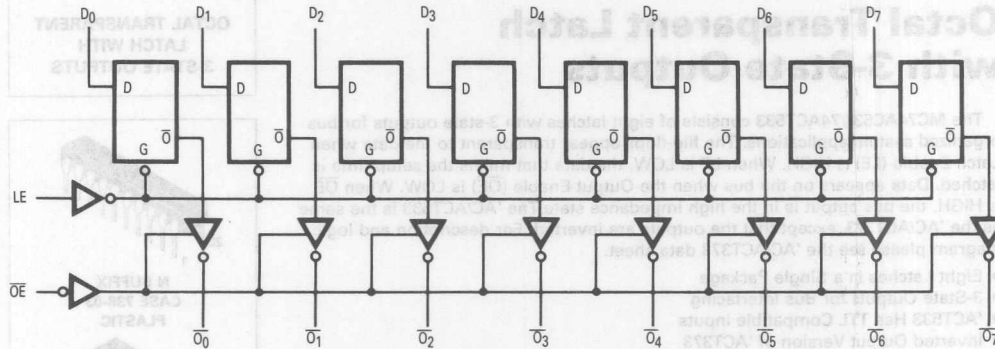


**DW SUFFIX
CASE 751D-03
PLASTIC**



MC74AC533 • MC74ACT533

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC533 • MC74ACT533

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) *AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V V _{CC} @ 4.5 V V _{CC} @ 5.5 V	150 40 25		ns/V
t _r , t _f	Input Rise and Fall Time (Note 2) *ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V V _{CC} @ 5.5 V	10 8.0		ns/V
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

- V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0		8.0 5.0				ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0		7.0 5.0				ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0		8.0 5.0				ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0		7.0 5.0				ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0		6.5 4.5				ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0		6.0 4.5				ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0				ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0		5.0 4.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0	3.5 2.0			ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0	-2.5 -1.5			ns	3-9
t _w	LE Pulse Width, HIGH	3.3 5.0	3.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
tPLH	Propagation Delay Dn to On	5.0						ns	3-5
tPHL	Propagation Delay Dn to On	5.0						ns	3-5
tPLH	Propagation Delay LE to On	5.0						ns	3-6
tPHL	Propagation Delay LE to On	5.0						ns	3-6
tPZH	Output Enable Time	5.0						ns	3-7
tPZL	Output Enable Time	5.0						ns	3-8
tPHZ	Output Disable Time	5.0						ns	3-7
tPLZ	Output Disable Time	5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	5.0				ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	5.0				ns	3-9
t _w	LE Pulse Width, HIGH	5.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance		pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance		pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

**MC74AC534
MC74ACT534**

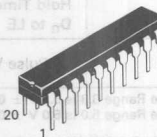
Product Preview

Octal D-Type Flip-Flop With State-Outputs

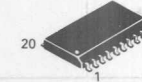
The MC74AC534/74ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'AC/ACT534 is the same as the 'AC/ACT374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus Oriented Applications

OCTAL D-TYPE
FLIP-FLOP WITH
3-STATE OUTPUTS

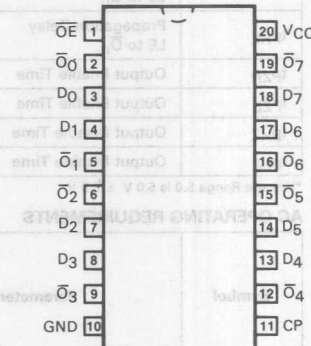
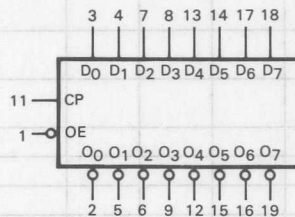


N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL



PIN NAMES

D₀-D₇ Data Inputs
CP Clock Pulse Input
OE 3-State Output Enable Input
O₀-O₇ Complementary 3-State Outputs

Symbol	Parameter	Units	Test Conditions
C _{in}	Input Capacitance	pf	V _{CC} = 5.0 V
C _o	Output Capacitance	pf	V _{CC} = 5.0 V

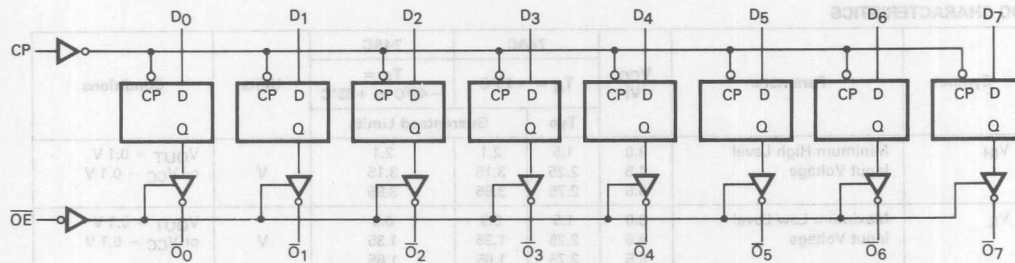
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FACT DATA

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MC74AC534 • MC74ACT534

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC534/74ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-

to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

FACT DATA

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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Symbol	Parameter	Units	Typ	Max
V _{CC}	Supply Voltage	V	5.0	5.5
V _{IN}	DC Input Voltage, Output Voltage (ref. to GND)	V	0	5.5
t _r	Input Rise and Fall Time (Note 1) *AC Devices except Schmitt inputs	nsV	150	150
			40	40
			25	25
			10	10
t _f	Input Rise and Fall Time (Note 2) *AC Devices except Schmitt inputs	nsV	150	150
			40	40
			25	25
			10	10
T _J	Junction Temperature (T _{DP})	°C	140	140
T _A	Operating Ambient Temperature Range	°C	55	55
I _{OH}	Output Current — High	mA	-25	-25
I _{OL}	Output Current — Low	mA	25	25

FACT DATA

MC74AC534 • MC74ACT534

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC534 • MC74ACT534

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0						MHz	3-3
t _{PLH}	Propagation Delay CP to \overline{O}_n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CP to \overline{O}_n	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time \overline{OE} to \overline{O}_n	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time \overline{OE} to \overline{O}_n	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time \overline{OE} to \overline{O}_n	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time \overline{OE} to \overline{O}_n	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0					ns	3-9
t _w	CP Pulse Width HIGH or LOW	3.3 5.0					ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC534 • MC74ACT534

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0		100		120		MHz	3-3
t _{PLH}	Propagation Delay CP to \bar{O}_n	5.0	2.5	6.5	11.5	2.0	12.5	ns	3-6
t _{PHL}	Propagation Delay CP to \bar{O}_n	5.0	2.0	6.0	10.5	2.0	12	ns	3-6
t _{PZH}	Output Enable Time $\bar{O}E$ to \bar{O}_n	5.0	2.5	6.5	12	2.0	12.5	ns	3-7
t _{PZL}	Output Enable Time $\bar{O}E$ to \bar{O}_n	5.0	2.0	6.0	11	2.0	11.5	ns	3-8
t _{PHZ}	Output Disable Time $\bar{O}E$ to \bar{O}_n	5.0	1.5	7.0	12.5	1.0	13.5	ns	3-7
t _{PLZ}	Output Disable Time $\bar{O}E$ to \bar{O}_n	5.0	1.5	5.5	10.5	1.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	1.0	3.5	4.0	ns	3-9
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	−1.0	1.0	1.5	ns	3-9
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V



MOTOROLA

**MC74AC540
MC74ACT540
MC74AC541
MC74ACT541**

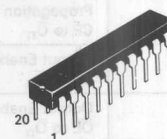
Octal Buffer/Line Driver with 3-State Outputs

The MC74AC540/74ACT540 and MC74AC541/74ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The MC74AC541/74ACT541 is a noninverting option of the MC74AC540/74ACT540.

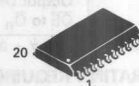
These devices are similar in function to the MC74AC240/74ACT240 and MC74AC244/74ACT244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

- 3-State Outputs
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Outputs Source/Sink 24 mA
- MC74AC540/74ACT540 Provides Inverted Outputs
- MC74AC541/74ACT541 Provides Noninverted Outputs
- 'ACT540 and 'ACT541 Have TTL Compatible Inputs

**OCTAL
BUFFER/LINE DRIVER
WITH 3-STATE
OUTPUTS**

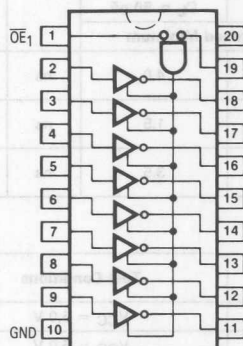


**N SUFFIX
CASE 738-03
PLASTIC**

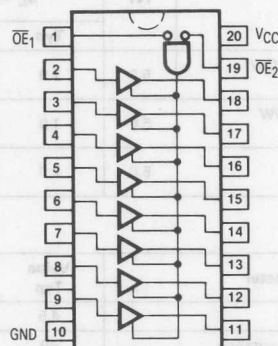


**DW SUFFIX
CASE 751D-03
PLASTIC**

MC74AC540/74ACT540



MC74AC541/74ACT541



TRUTH TABLE

Inputs			Outputs	
OE ₁	OE ₂	D	'540	'541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

FACT DATA

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC540 • MC74ACT540 • MC74AC541 • MC74ACT541

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC540 • MC74ACT540 • MC74AC541 • MC74ACT541

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC540 • MC74ACT540 • MC74AC541 • MC74ACT541

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output ('AC540)	3.3 5.0	1.5 1.5	5.5 4.0	7.5 6.0	1.0 1.0	8.0 6.5	ns	3-5
t _{PHL}	Propagation Delay Data to Output ('AC540)	3.3 5.0	1.5 1.5	5.0 4.0	7.0 5.5	1.0 1.0	7.5 6.0	ns	3-5
t _{PZH}	Output Enable Time ('AC540)	3.3 5.0	3.0 2.0	8.5 6.5	11 8.5	2.5 2.0	12 9.5	ns	3-7
t _{PZL}	Output Enable Time ('AC540)	3.3 5.0	2.5 2.0	7.5 6.0	10 7.5	2.0 1.5	11 8.5	ns	3-8
t _{PHZ}	Output Disable Time ('AC540)	3.3 5.0	2.5 1.5	8.5 7.5	13 10.5	1.5 1.0	14 11	ns	3-7
t _{PLZ}	Output Disable Time ('AC540)	3.3 5.0	2.5 1.5	7.0 6.0	10 8.0	2.0 1.5	11 9.0	ns	3-8
t _{PLH}	Propagation Delay Data to Output ('AC541)	3.3 5.0	2.0 1.5	5.5 4.0	8.0 6.0	1.5 1.0	9.0 6.5	ns	3-5
t _{PHL}	Propagation Delay Data to Output ('AC541)	3.3 5.0	2.0 1.5	5.5 4.0	8.0 6.0	1.5 1.0	8.5 6.5	ns	3-5
t _{PZH}	Output Enable Time ('AC541)	3.3 5.0	3.0 2.0	8.0 6.0	11.5 8.5	3.0 1.5	12.5 9.5	ns	3-7
t _{PZL}	Output Enable Time ('AC541)	3.3 5.0	2.5 1.5	7.0 5.5	10 7.5	2.5 1.0	11.5 8.5	ns	3-8
t _{PHZ}	Output Disable Time ('AC541)	3.3 5.0	3.5 2.0	9.0 7.0	12.5 9.5	2.5 1.0	14 10.5	ns	3-7
t _{PLZ}	Output Disable Time ('AC541)	3.3 5.0	2.5 2.0	6.5 5.5	9.5 7.5	2.0 1.0	10.5 8.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC540 • MC74ACT540 • MC74AC541 • MC74ACT541

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Data to Output ('ACT540)	5.0	1.0		7.0	1.0	7.5	ns	3-5
t _{PHL}	Propagation Delay Data to Output ('ACT540)	5.0	1.0		8.0	1.0	8.5	ns	3-5
t _{PZH}	Output Enable Time (ACT540)	5.0	1.0		10.5	1.0	11.5	ns	3-7
t _{PZL}	Output Enable Time (ACT540)	5.0	1.0		9.5	1.0	10.5	ns	3-8
t _{PHZ}	Output Disable Time (ACT540)	5.0	1.0		12	1.0	12.5	ns	3-7
t _{PLZ}	Output Disable Time (ACT540)	5.0	1.0		9.0	1.0	10	ns	3-8
t _{PLH}	Propagation Delay Data to Output ('ACT541)	5.0	1.5		7.0	1.0	7.5	ns	3-5
t _{PHL}	Propagation Delay Data to Output ('ACT541)	5.0	1.5		8.0	1.0	8.5	ns	3-5
t _{PZH}	Output Enable Time (ACT541)	5.0	2.0		10.5	1.0	11.5	ns	3-7
t _{PZL}	Output Enable Time (ACT541)	5.0	1.5		9.5	1.0	10.5	ns	3-8
t _{PHZ}	Output Disable Time (ACT541)	5.0	2.0		12	1.0	12.5	ns	3-7
t _{PLZ}	Output Disable Time (ACT541)	5.0	2.0		9.0	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

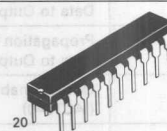
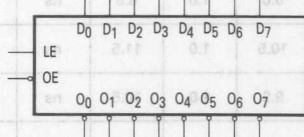
Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V

**MOTOROLA****MC74AC563
MC74ACT563****Octal D-Type Latch
with 3-State Outputs**

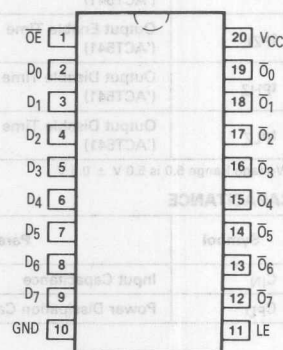
The MC74AC563/74ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

The MC74AC563/74ACT563 device is functionally identical to the MC74AC573/74ACT573, but with inverted outputs.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC573/74ACT573 but with Inverted Outputs
- Outputs Source/Sink 24 mA
- 'ACT563 Has TTL Compatible Inputs

**OCTAL D-TYPE
LATCH WITH
3-STATE OUTPUTS****N SUFFIX
CASE 738-03
PLASTIC****DW SUFFIX
CASE 751D-03
PLASTIC****LOGIC SYMBOL****PIN NAMES**

D ₀ -D ₇	Data Inputs	Units	Value
LE	Latch Enable Input		
OE	3-State Output Enable Input		
O ₀ -O ₇	3-State Latch Outputs		



MC74AC563 • MC74ACT563

FUNCTIONAL DESCRIPTION

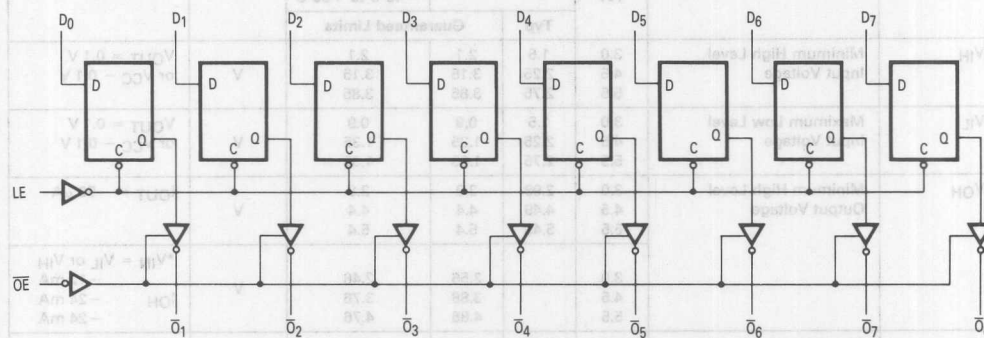
The MC74AC563/74ACT563 contains eight D-type latches with 3-state complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
\overline{OE}	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

FACT DATA

MC74AC563 • MC74ACT563

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC 2.0	5.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	'ACT 4.5	5.0	5.5	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V 150			ns/V
		V _{CC} @ 4.5 V 40			
		V _{CC} @ 5.5 V 25			
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V 10			ns/V
		V _{CC} @ 5.5 V 8.0			
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC563 • MC74ACT563

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to \bar{O}_n	3.3 5.0						ns	3-5
t _{PHL}	Propagation Delay D _n to \bar{O}_n	3.3 5.0						ns	3-5
t _{PLH}	Propagation Delay LE to \bar{O}_n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay LE to \bar{O}_n	3.3 5.0						ns	3-6
t _{pZH}	Output Enable Time	3.3 5.0						ns	3-7
t _{pZL}	Output Enable Time	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC563 • MC74ACT563

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0				ns	3-9
t _w	LE Pulse Width, HIGH	3.3 5.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to \bar{O}_n	5.0	3.0		11.5	2.5	12.5	ns	3-5
t _{PHL}	Propagation Delay D _n to \bar{O}_n	5.0	3.0		10	2.5	11	ns	3-5
t _{PLH}	Propagation Delay LE to \bar{O}_n	5.0	3.0		10.5	2.5	11.5	ns	3-6
t _{PHL}	Propagation Delay LE to \bar{O}_n	5.0	2.5		9.5	2.0	10.5	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.5		9.0	2.0	10	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0		8.5	2.0	9.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	3.5		10.5	2.5	11.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	2.0		8.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	5.0		4.0	4.5	ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	5.0		0	0	ns	3-9
t _w	LE Pulse Width, HIGH	5.0		3.0	3.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

MC74AC564 MC74ACT564

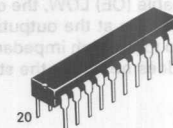
Octal D-Type Latch with 3-State Outputs

The MC74AC564/74ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

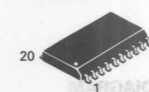
The MC74AC564/74ACT564 device is functionally identical to the MC74AC574/74ACT574, but with inverted outputs.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC574/74ACT574 but with Inverted Outputs
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT564 Has TTL Compatible Inputs

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUTS

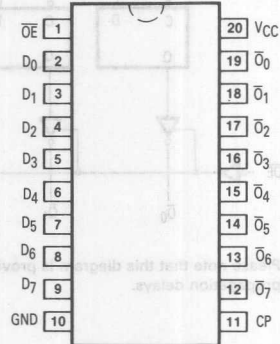
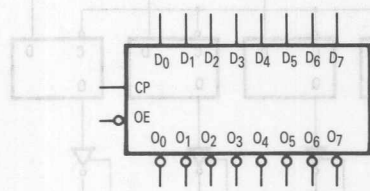


**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**

LOGIC SYMBOL



PIN NAMES

- D₀-D₇ Data Inputs
CP Clock Pulse Input
OE 3-State Output Enable Input
Q₀-Q₇ 3-State Outputs

Symbol	Parameter	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	V
V _{IN}	DC Input Voltage (Referenced to GND)	V
V _{OUT}	DC Output Voltage (Referenced to GND)	V
I _{IN}	DC Input Current per Pin	mA
I _{OUT}	DC Output Sink/Source Current per Pin	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	mA
T _{STG}	Storage Temperature	°C

FACT DATA

5-269

FUNCTIONAL DESCRIPTION

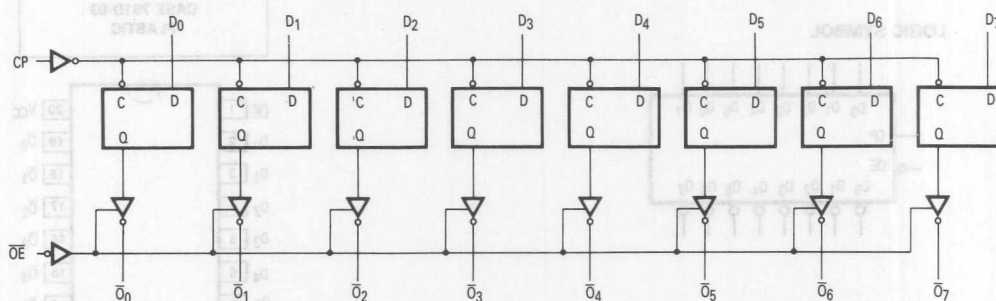
The MC74AC564/74ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	\downarrow	L	H	Z	Load
H	\downarrow	H	L	Z	Load
L	\downarrow	L	H	H	Data Available
L	\downarrow	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 \downarrow = LOW-to-HIGH Transition
 NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

FACT DATA

MC74AC564 • MC74ACT564

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC564 • MC74ACT564

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0						MHz	3-3
t _{PLH}	Propagation Delay CP to \bar{O}_n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CP to \bar{O}_n	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC564 • MC74ACT564



AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0				ns	3-9
t _w	CP Pulse Width HIGH or LOW	3.3 5.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	85			75		MHz	3-3
t _{PLH}	Propagation Delay CP to O _n	5.0	2.0		10.5	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay CP to O _n	5.0	1.5		9.5	1.5	10.5	ns	3-6
t _{PZH}	Output Enable Time	5.0	1.5		9.0	1.5	9.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5		8.5	1.0	9.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5		10.5	1.5	11.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5		8.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0		2.5	3.0	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0		1.0	1.0	ns	3-9	
t _w	LE Pulse Width HIGH or LOW	5.0		3.0	3.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V

FACT DATA

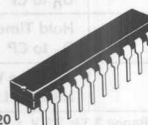
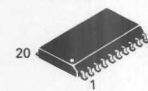
**MOTOROLA**

Product Preview

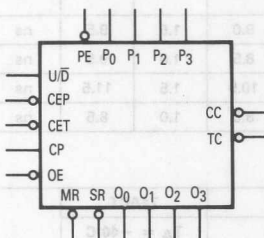
4-Bit Bidirectional Counters with 3-State Outputs

The MC74AC568 and MC74AC569 are fully synchronous, bidirectional counters with 3-state outputs. The MC74AC568 is a BCD decade counter; the MC74AC569 is a modulo 16 binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/D input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry (CC) and Terminal Count (TC) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable (OE) input forces the output buffers into the high-impedance state but does not prevent counting, resetting or parallel loading.

- Synchronous Counting and Loading
- Lookahead Carry Capability for Easy Cascading
- Preset Capability for Programmable Operation
- 3-State Outputs for Bus Organized Systems
- Outputs Source/Sink 24 mA
- Synchronous and Asynchronous Resets

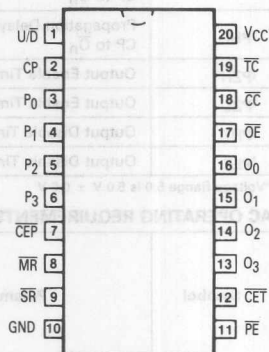
**MC74AC568
MC74AC569****4-BIT BIDIRECTIONAL
COUNTERS WITH
3-STATE OUTPUTS****N SUFFIX
CASE 738-03
PLASTIC****DW SUFFIX
CASE 751D-03
PLASTIC**

LOGIC SYMBOL

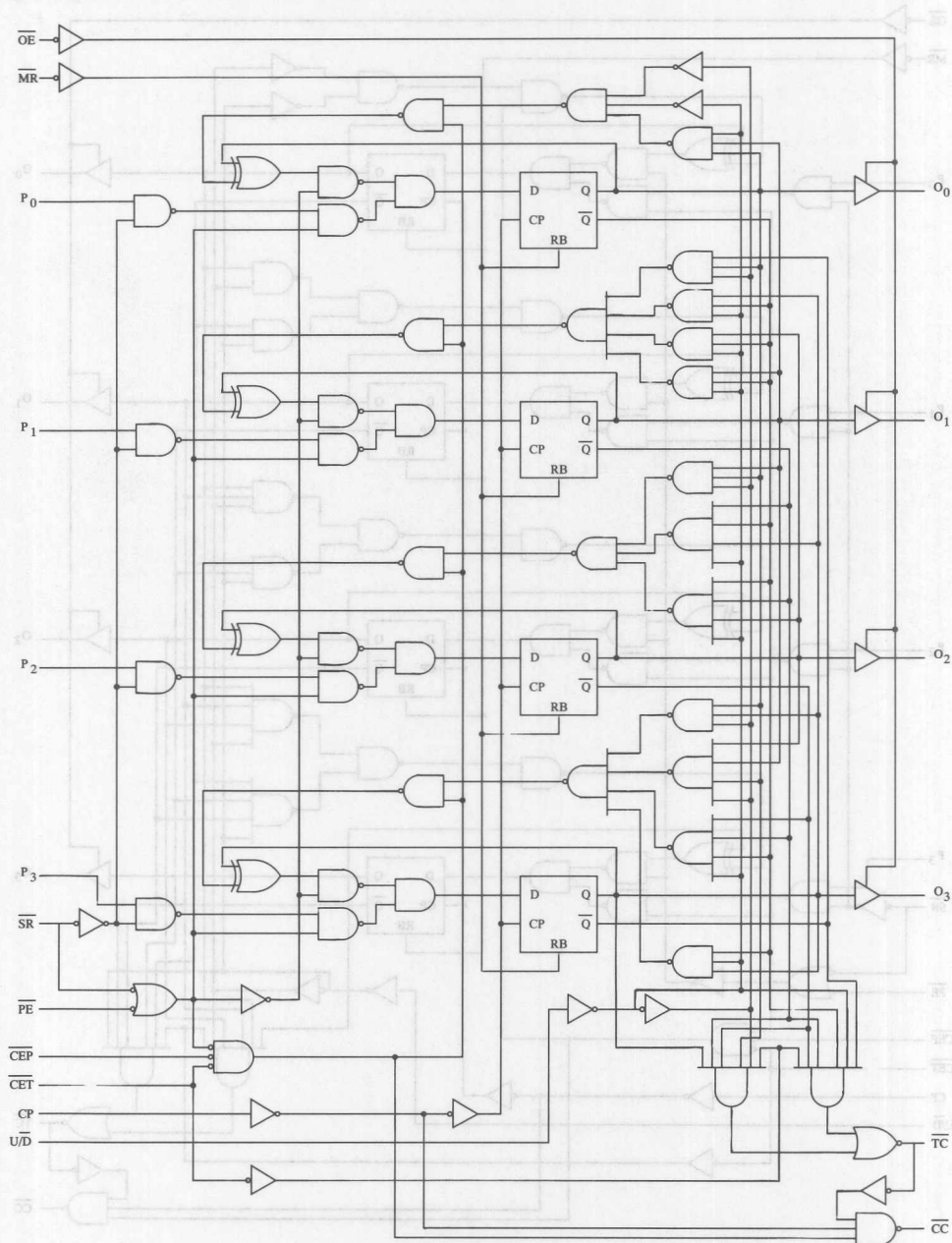


PIN NAMES

P ₀ -P ₃	Parallel Data Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
PE	Parallel Enable Input
U/D	Up/Down Count Control Input
OE	Output Enable Input
MR	Master Reset Input
SR	Synchronous Reset Input
O ₀ -O ₃	3-State Parallel Data Outputs
TC	Terminal Count Output
CC	Clocked Carry Output



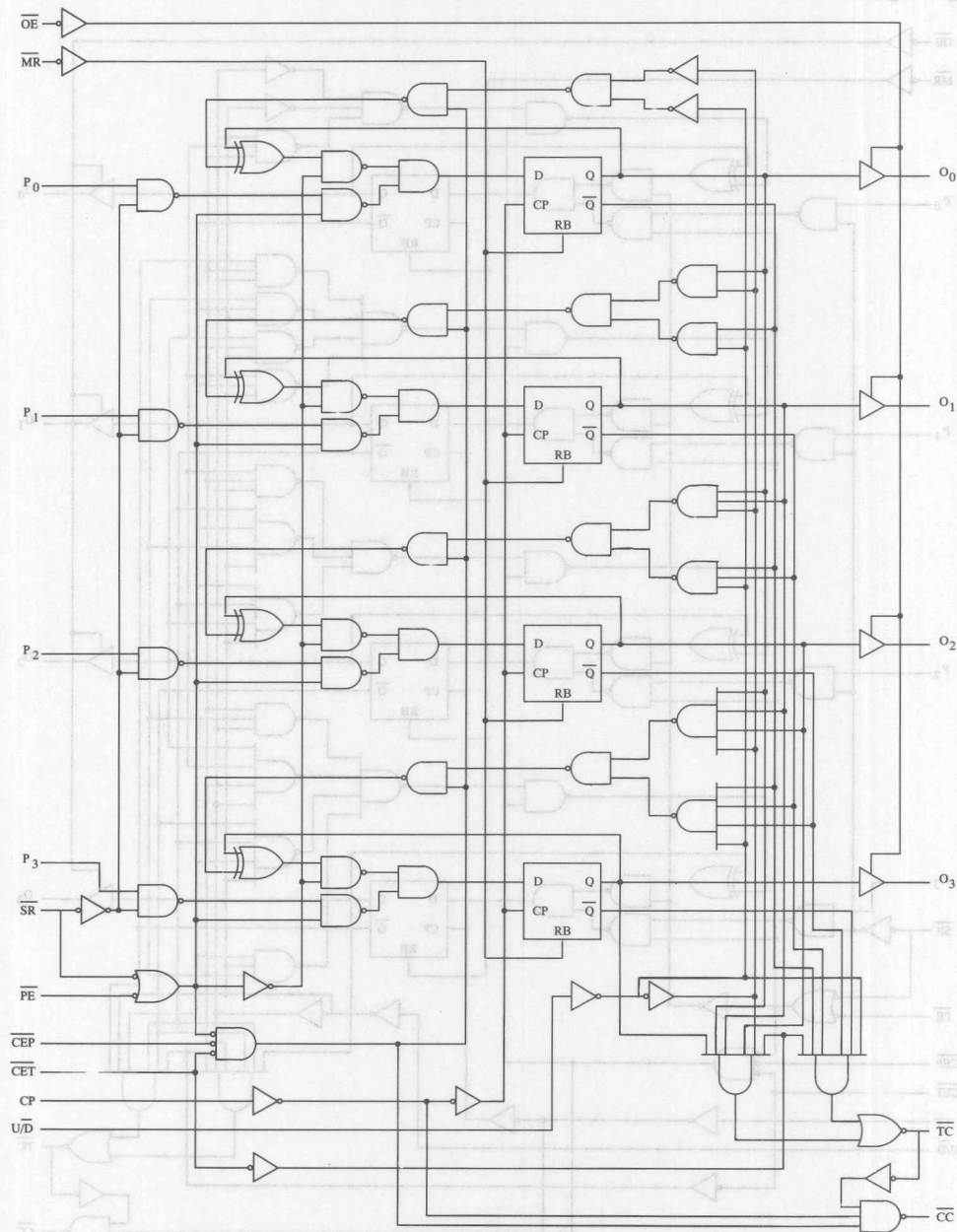
Logic Diagram (AC568)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC568 • MC74AC569

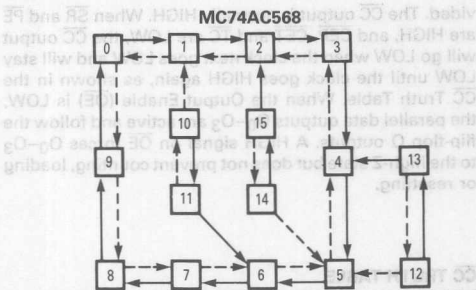
Logic Diagram (AC569)



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

STATE DIAGRAMS



Inputs	SR	PE	CET	CEP	TC	Outputs
Count Down	---	---	---	---	---	---
Count Up	---	---	---	---	---	---
0	L	X	X	X	X	L
1	L	X	X	X	X	H
2	L	X	X	X	X	H
3	L	X	X	X	X	H
4	L	X	X	X	X	H
5	L	X	X	X	X	H
6	L	X	X	X	X	H
7	L	X	X	X	X	H
8	L	X	X	X	X	H
9	L	X	X	X	X	H

LOGIC EQUATIONS:

Count Enable = $\overline{\text{CEP}} \cdot \overline{\text{CET}} \cdot \text{PE}$

Up ('AC568): $\overline{\text{TC}} = \overline{\text{Q}_0} \cdot \overline{\text{Q}_1} \cdot \overline{\text{Q}_2} \cdot \overline{\text{Q}_3} \cdot (\text{Up}) \cdot \text{CET}$

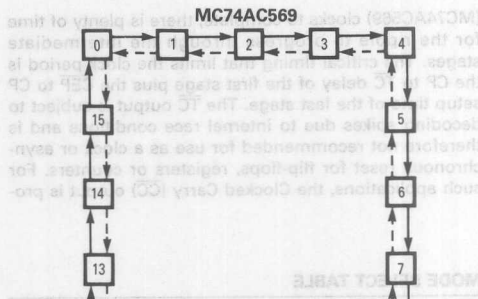
('AC569): $\overline{\text{TC}} = \overline{\text{Q}_0} \cdot \overline{\text{Q}_1} \cdot \overline{\text{Q}_2} \cdot \overline{\text{Q}_3} \cdot (\text{Up}) \cdot \text{CET}$

Down (Both): $\overline{\text{TC}} = \overline{\text{Q}_0} \cdot \overline{\text{Q}_1} \cdot \overline{\text{Q}_2} \cdot \overline{\text{Q}_3} \cdot (\text{Down}) \cdot \text{CET}$

FUNCTIONAL DESCRIPTION

The MC74AC568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The MC74AC569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset (MR), Synchronous Reset (SR), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — plus the Up/Down (U/D) input determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_N) inputs to be loaded into the flip-flops on the next rising edge of CP. With MR, SR and PE HIGH, CEP and CET permit counting when both are LOW. Conversely, a HIGH signal on either CEP or CET inhibits counting.



Inputs	SR	PE	CET	CEP	TC	Outputs
Count Down	---	---	---	---	---	---
Count Up	---	---	---	---	---	---
0	L	X	X	X	X	L
1	L	X	X	X	X	H
2	L	X	X	X	X	H
3	L	X	X	X	X	H
4	L	X	X	X	X	H
5	L	X	X	X	X	H
6	L	X	X	X	X	H
7	L	X	X	X	X	H
8	L	X	X	X	X	H
9	L	X	X	X	X	H
10	L	X	X	X	X	H
11	L	X	X	X	X	H
12	L	X	X	X	X	H
13	L	X	X	X	X	H
14	L	X	X	X	X	H
15	L	X	X	X	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Indifferent

the MC74AC568 and MC74AC569 use edge-triggered flip-flops and changing the SR, PE, CEP, CET or U/D inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally HIGH and goes LOW providing CET is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the MC74AC568, 15 for the MC74AC569) in the Up mode. TC will then remain LOW until a state change occurs, whether by counting or presetting, or until U/D or CET is changed. To implement synchronous multistage counters, the connections between the TC output and the CEP and CET inputs can provide either slow or fast carry propagation. Figure a shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure b are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 (MC74AC568) or 16

MODE SELECT TABLE

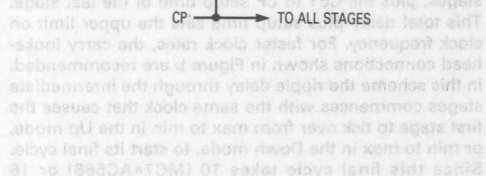
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H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CC TRUTH TABLE

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* = TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



MC74AC568 • MC74AC569

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC568 • MC74AC569

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} , V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC568 • MC74AC569

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0						MHz	3-3
t _{PLH}	Propagation Delay CP to O _n (PE HIGH or LOW)	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CP to O _n (PE HIGH or LOW)	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay U/D to TC (*568)	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay U/D to TC (*568)	3.3 5.0						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS — continued (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay U/D to TC ('569)	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay U/D to TC ('569)	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay CP to CC	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CP to CC	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay CEP or CET to CC	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CEP or CET to CC	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay MR to O _n	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0						ns	3-7
t _{PZL}	Output Disable Time OE to O _n	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC568 • MC74AC569



AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0				ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0				ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0				ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0				ns	3-9	
t _s	Setup Time, HIGH or LOW PE to CP	3.3 5.0				ns	3-9	
t _h	Hold Time, HIGH or LOW PE to CP	3.3 5.0				ns	3-9	
t _s	Setup Time, HIGH or LOW U/D to CP ('568)	3.3 5.0				ns	3-9	
t _s	Setup Time, HIGH or LOW U/D to CP ('569)	3.3 5.0				ns	3-9	
t _h	Hold Time, HIGH or LOW U/D to CP	3.3 5.0				ns	3-9	
t _s	Setup Time, HIGH or LOW SR to CP	3.3 5.0				ns	3-9	
t _h	Hold Time, HIGH or LOW SR to CP	3.3 5.0				ns	3-9	
t _w	CP Pulse Width HIGH or LOW	3.3 5.0				ns	3-6	
t _w	MR Pulse Width, LOW	3.3 5.0				ns	3-6	
t _{rec}	MR Recovery Time	3.3 5.0				ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance		pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance		pF	V _{CC} = 5.0 V



MOTOROLA

**MC74AC573
MC74ACT573**

Octal D-Type Latch with 3-State Outputs

The MC74AC573/74ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

The MC74AC573/74ACT573 is functionally identical to the MC74AC373/74ACT373 but has inputs and outputs on opposite sides.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC373/74ACT373
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- ACT573 Has TTL Compatible Inputs

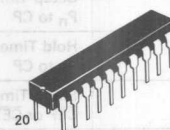
LOGIC SYMBOL



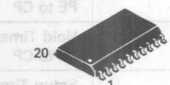
PIN NAMES

D₀-D₇ Data Inputs
LE Latch Enable Input
 \overline{OE} 3-State Output Enable Input
O₀-O₇ 3-State Latch Outputs

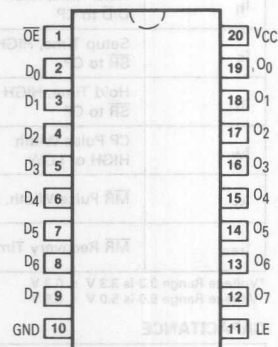
**OCTAL D-TYPE
LATCH WITH
3-STATE OUTPUTS**



**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**



TRUTH TABLE

Inputs			Outputs
\overline{OE}	LE	D	O _n
L	H	H	H
L	H	L	H
L	L	X	O ₀
H	X	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O₀ = Previous O₀ before LOW-to-HIGH Transition of Clock

FACT DATA

preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are enabled. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.



and not be used to estimate

Value	Unit
-0.5 to +7.0	V
-0.5 to $V_{CC} + 0.5$	V
-0.5 to $V_{CC} + 0.5$	V
± 20	mA
± 50	mA
± 50	mA
-65 to +150	°C

should be restricted to the Recommended

MC74AC573 • MC74ACT573

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
		4.5	5.0	5.5	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} = −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC573 • MC74ACT573

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0						ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0						ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC573 • MC74ACT573

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0					ns	3-9
t _w	LE Pulse Width, HIGH	3.3 5.0					ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _N to O _N	5.0	2.5		10.5	2.0	12	ns	3-5
t _{PHL}	Propagation Delay D _N to O _N	5.0	2.5		10.5	2.0	12	ns	3-5
t _{PLH}	Propagation Delay LE to O _N	5.0	3.0		10.5	2.5	12	ns	3-6
t _{PHL}	Propagation Delay LE to O _N	5.0	2.5		9.5	2.0	10.5	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.0		10	1.5	11	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5		9.5	1.5	10.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	2.5		11	1.5	12.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5		8.5	1.0	9.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	5.0		3.0		3.5	ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	5.0		0		0	ns	3-9
t _w	LE Pulse Width, HIGH	5.0		3.5		4.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	25	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

MC74AC574 MC74ACT574

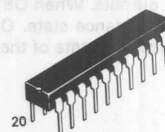
Octal D-Type Flip-Flop with 3-State Outputs

The MC74AC574/74ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

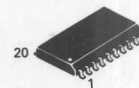
The MC74AC574/74ACT574 is functionally identical to the MC74AC374/74ACT374 except for the pinouts.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC374/74ACT374
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT574 Has TTL Compatible Inputs

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

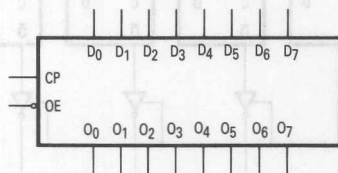


**N SUFFIX
CASE 738-03
PLASTIC**



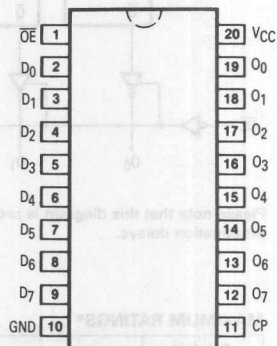
**DW SUFFIX
CASE 751D-03
PLASTIC**

LOGIC SYMBOL



PIN NAMES

- D₀-D₇ Data Inputs
CP Clock Pulse Input
OE 3-State Output Enable Input
Q₀-Q₇ 3-State Outputs



FUNCTIONAL DESCRIPTION

The MC74AC574/74ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O_n	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	\downarrow	L	L	Z	Load
H	\downarrow	H	H	Z	Load
L	\downarrow	L	L	L	Data Available
L	\downarrow	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level

L = LOW Voltage Level

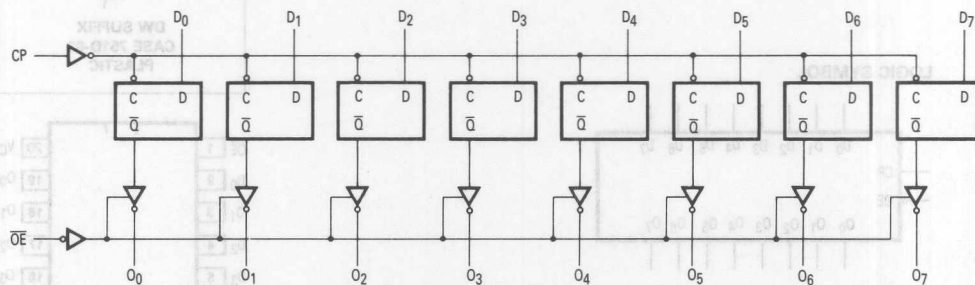
X = Immaterial

Z = High Impedance

 \downarrow = LOW-to-HIGH Clock Transition

NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC574 • MC74ACT574

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = - 50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} = - 24 mA - 24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		± 0.5	± 5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			- 75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC574 • MC74ACT574

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	75 95			60 85		MHz	3-3
t _{PLH}	Propagation Delay CP to O _N	3.3 5.0	3.5 2.0		13.5 9.5	3.5 2.0	15 11	ns	3-6
t _{PHL}	Propagation Delay CP to O _N	3.3 5.0	3.5 2.0		12 8.5	3.5 2.0	13.5 9.5	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	2.5 2.0		11 8.5	2.5 2.0	12 9.0	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	3.0 1.5		10.5 8.0	3.5 2.0	11.5 9.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	4.0 2.0		12 9.5	4.5 2.0	13 10.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5		9.0 7.5	2.5 1.5	10 8.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC574 • MC74ACT574

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3		2.5	3.0	ns	3-9	
		5.0		1.5	2.0			
t _h	Hold Time, HIGH or LOW D _n to CP	3.3		1.5	1.5	ns	3-9	
		5.0		1.5	1.5			
t _w	CP Pulse Width HIGH or LOW	3.3		6.0	7.0	ns	3-6	
		5.0		4.0	5.0			

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74ACT			74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	100			85		ns	3-3
tPLH	Propagation Delay CP to ON	5.0	2.5		11	2.0	12	ns	3-6
tPHL	Propagation Delay CP to ON	5.0	2.0		10	1.5	11	ns	3-6
tPZH	Output Enable Time	5.0	2.0		9.5	1.5	10	ns	3-7
tPZL	Output Enable Time	5.0	2.0		9.0	1.5	10	ns	3-8
tPHZ	Output Disable Time	5.0	2.0		10.5	1.5	11.5	ns	3-7
tPLZ	Output Disable Time	5.0	2.0		8.5	1.5	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0		2.5	2.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0		1.0	1.0	ns	3-9	
t _w	CP Pulse Width HIGH or LOW	5.0		3.0	4.0	ns	3-6	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

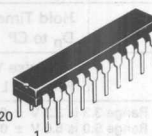
MC74AC620 MC74ACT620

Octal Bidirectional Transceiver with 3-State Outputs

The MC74AC620/74ACT620 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/\bar{R} = HIGH, or from bus B to bus A when T/\bar{R} = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source - 24 mA
- 'ACT620 Has TTL Compatible Inputs

OCTAL BIDIRECTIONAL
TRANSCEIVER WITH
3-STATE OUTPUTS



N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

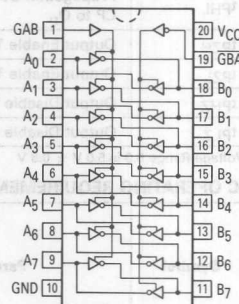
PIN NAMES

A₀-A₇ Side A Inputs or 3-State Outputs
GAB Enable B Outputs
GBA Enable A Outputs
B₀-B₇ Side B Inputs or 3-State Outputs

TRUTH TABLE

GAB	GBA	Applied Inputs	Valid Direction I/P→O/P	Output
H	H	H	\bar{A} to B	L
H	H	L	\bar{A} to B	H
L	L	H	B to A	L
L	L	L	B to A	H

H = HIGH Voltage Level
L = LOW Voltage Level



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} at 3.0 V are guaranteed to be less than or equal to the respective limit at 5.5 V V_{CC}.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

3-3	ns	1.50	1.0	10.0	5.5	1.5	5.0	Output Enable Time
3-3	ns	1.50	1.0	10.0	5.5	1.5	5.0	Output Disable Time
3-1	ns	11.0	1.0	10.0	5.5	1.5	5.0	Output Enable Time
3-2	ns	11.0	1.0	10.0	5.5	1.5	5.0	Output Disable Time

*Voltage Range 5.0 ± 0.2 V ± 0.2 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{IO}	Input/Output Capacitance	14	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	55	pF	V _{CC} = 5.0 V

MC74AC620 • MC74ACT620

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.5	1.0 1.0	9.5 7.5	ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.0	1.0 1.0	9.5 7.0	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	8.0 6.0	11.5 8.5	2.0 1.0	13.0 9.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 1.5	8.5 6.5	12.0 9.0	2.0 1.0	13.5 10.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.0	12.0 9.0	1.0 1.0	13.0 10.0	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.5 6.5	12.0 9.0	1.5 1.0	13.0 10.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	5.0	1.5	3.5	7.5	1.0	8.5	ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	5.0	1.5	3.5	8.0	1.0	9.0	ns	3-5
t _{PZH}	Output Enable Time	5.0	1.5	6.0	10.0	1.0	11.0	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5	6.5	10.0	1.0	12.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5	6.0	10.0	1.0	11.0	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5	6.5	10.0	1.0	11.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V



MOTOROLA

MC74AC623 MC74ACT623

Octal Bidirectional Transceiver with 3-State Outputs

The MC74AC623/74ACT623 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when $T/\bar{R} = \text{HIGH}$, or from bus B to bus A when $T/\bar{R} = \text{LOW}$. The enable input can be used to disable the device so the buses are effectively isolated.

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source – 24 mA
- *ACT623 Has TTL Compatible Inputs

PIN NAMES

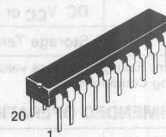
A₀–A₇ Side A Inputs or 3-State Outputs
GAB Enable B Outputs
 $\overline{\text{GBA}}$ Enable A Outputs
B₀–B₇ Side B Inputs or 3-State Outputs

TRUTH TABLE

GAB	$\overline{\text{GBA}}$	Applied Inputs	Valid Direction I/P→O/P	Output
H	H	H	A to B	H
H	H	L	A to B	L
L	L	H	B to A	H
L	L	L	B to A	L

H = HIGH Voltage Level
L = LOW Voltage Level

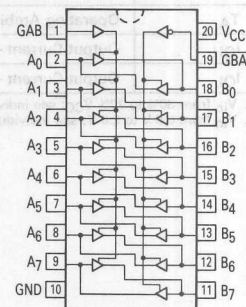
OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE OUTPUTS



N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.



Output	Input	Output	Input	Output	Input
H	A to B	H	H	H	H
L	A to B	L	H	H	L
H	B to A	H	L	L	H
L	B to A	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

MC74AC623 • MC74ACT623

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
			4.5		3.86	3.76		
			5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
			4.5		0.36	0.44		
			5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC623 • MC74ACT623

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC623 • MC74ACT623

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _N to B _N or B _N to A _N	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.5	1.0 1.0	9.5 7.5	ns	3-5
t _{PHL}	Propagation Delay A _N to B _N or B _N to A _N	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.0	1.0 1.0	9.5 7.0	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	8.0 6.0	11.5 8.5	2.0 1.0	13.0 9.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 1.5	8.5 6.5	12.0 9.0	2.0 1.0	13.5 10.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.0	12.0 9.0	1.0 1.0	13.0 10.0	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.5 6.5	12.0 9.0	1.5 1.0	13.0 10.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	5.0	1.5	3.5	7.5	1.0	8.5	ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	5.0	1.5	3.5	8.0	1.0	9.0	ns	3-5
t _{PZH}	Output Enable Time	5.0	1.5	6.0	10.0	1.0	11.0	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5	6.5	10.0	1.0	12.0	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5	6.0	10.0	1.0	11.0	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5	6.5	10.0	1.0	11.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15.0	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	60	pF	V _{CC} = 5.0 V

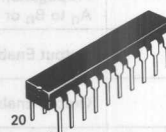
**MOTOROLA****MC74AC640
MC74ACT640**

Octal Bidirectional Transceiver with 3-State Outputs

**OCTAL BIDIRECTIONAL
TRANSCIVER WITH
3-STATE OUTPUTS**

The MC74AC640/74ACT640 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/\bar{R} = HIGH, or from bus B to bus A when T/\bar{R} = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source — 24 mA
- 'ACT640 Has TTL Compatible Inputs



**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**

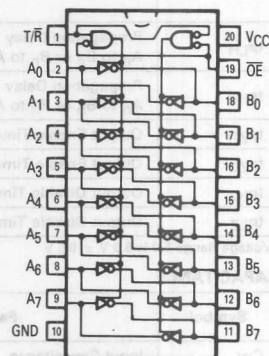
PIN NAMES

- A₀–A₇ Side A Inputs or 3-State Outputs
 OE Output Enable Input
 T/ \bar{R} Transmit/Receive Input
 B₀–B₇ Side B Inputs or 3-State Outputs

TRUTH TABLE

OE	T/ \bar{R}	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	L
L	L	L	B to A	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial



MC74AC640 • MC74ACT640

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} \approx 3.0$ V	150		ns/V
		$V_{CC} \approx 4.5$ V	40		
		$V_{CC} \approx 5.5$ V	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} \approx 4.5$ V	10		ns/V
		$V_{CC} \approx 5.5$ V	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
I _{IN}	Maximum Input Leakage Current	3.0	2.56	2.46	2.46	μA	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5	3.86	3.76	3.76			
		5.5	4.86	4.76	4.76			
I _{OZ}	Maximum 3-State Current	3.0	0.36	0.44	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5	0.36	0.44	0.44			
		5.5	0.36	0.44	0.44			
I _{OLD}	†Minimum Dynamic Output Current	5.5		75	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5		–75	–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	8.0	80	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC640 • MC74ACT640

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} = −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} = 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Output Enable Time	5.0	ns
Output Disable Time	5.0	ns
Output Enable Time	5.0	ns
Output Disable Time	5.0	ns

V_{OL} Range 0.0 to 0.5 V

Symbol	Parameter	Units	Typ
C _{IN}	Input Capacitance	pF	4.5
C _{IO}	Output Capacitance	pF	15
C _{PD}	Power Dissipation Capacitance	pF	45

FACT DATA

MC74AC640 • MC74ACT640

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.5	1.0 1.0	9.5 7.5	ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.5	1.0 1.0	9.5 7.5	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	8.0 6.0	11.5 8.0	2.0 1.0	12.5 9.0	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 1.5	8.5 6.5	12.5 9.5	2.0 1.0	13.5 10.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.0	12.0 9.0	1.0 1.0	12.5 10.0	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.5 6.5	12.0 9.5	1.5 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	5.0						ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	5.0						ns	3-5
t _{PZH}	Output Enable Time	5.0						ns	3-7
t _{PZL}	Output Enable Time	5.0						ns	3-8
t _{PHZ}	Output Disable Time	5.0						ns	3-7
t _{PLZ}	Output Disable Time	5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CI/O	Input/Output Capacitance	15	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	45	pF	VCC = 5.0 V

**MOTOROLA****MC74AC643
MC74ACT643**

Octal Bidirectional Transceiver with 3-State Outputs

The MC74AC643/74ACT643 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/\bar{R} = HIGH, or from bus B to bus A when T/\bar{R} = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source – 24 mA
- 'ACT643 Has TTL Compatible Inputs

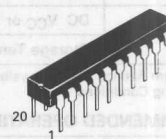
PIN NAMES

A₀–A₇ Side A Inputs or 3-State Outputs
 OE Output Enable Input
 T/ \bar{R} Transmit/Receive Input
 B₀–B₇ Side B Inputs or 3-State Outputs

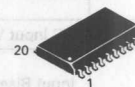
TRUTH TABLE

OE	T/ \bar{R}	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	\bar{A} to B	L
L	H	L	\bar{A} to B	H
L	L	H	B to A	H
L	L	L	B to A	L

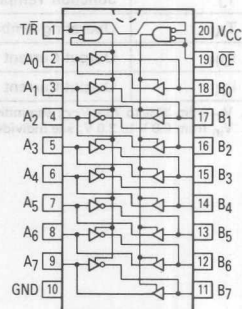
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

**OCTAL BIDIRECTIONAL
TRANSCEIVER WITH
3-STATE OUTPUTS**

**N SUFFIX
CASE 738-03
PLASTIC**



**DW SUFFIX
CASE 751D-03
PLASTIC**



FACT DATA

5-309

MC74AC643 • MC74ACT643

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	- 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	150		ns/V
		$V_{CC} @ 4.5 V$	40		
		$V_{CC} @ 5.5 V$	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	10		ns/V
		$V_{CC} @ 5.5 V$	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	- 40	25	85	°C
I_{OH}	Output Current — High			- 24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GN} D V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: IIN and ICC @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V VCC.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} – 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	3.3 5.0	1.5 1.5		5.0 3.5	1.0 1.0	9.5 7.5	ns	3-5
t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	3.3 5.0	1.5 1.5		5.0 3.5	1.0 1.0	9.5 7.5	ns	3-5
t _{PZH}	Output Enable Time	3.3 5.0	2.5 1.5		8.0 6.0	2.0 1.0	13.5 10.0	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 1.5		8.5 6.0	2.0 1.0	13.5 10.0	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	2.0 1.5		8.0 6.0	1.0 1.0	12.5 10.0	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5		8.5 6.5	1.5 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _N to B _N or B _N to A _N	5.0						ns	3-5
t _{PHL}	Propagation Delay A _N to B _N or B _N to A _N	5.0						ns	3-5
t _{PZH}	Output Enable Time	5.0						ns	3-7
t _{PZL}	Output Enable Time	5.0						ns	3-8
t _{PHZ}	Output Disable Time	5.0						ns	3-7
t _{PLZ}	Output Disable Time	5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	60	pF	V _{CC} = 5.0 V



FACT DATA



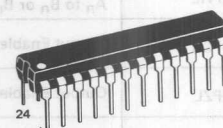
MOTOROLA

**MC74AC646
MC74ACT646**

Octal Transceiver/Register with 3-State Outputs (Non-Inverting)

The MC74AC646/74ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

**OCTAL
TRANSCIVER/REGISTER
WITH 3-STATE OUTPUTS
(NON-INVERTING)**



**N SUFFIX
CASE 724-03
PLASTIC**

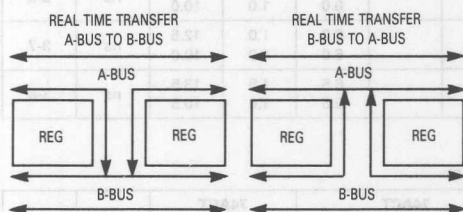


Figure 1

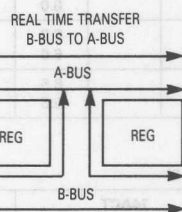


Figure 2

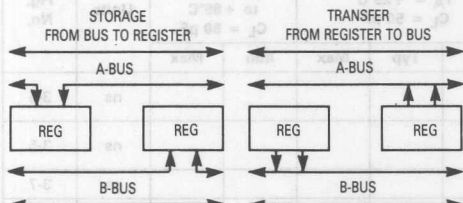


Figure 3

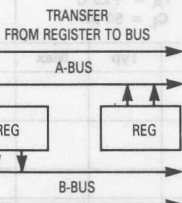
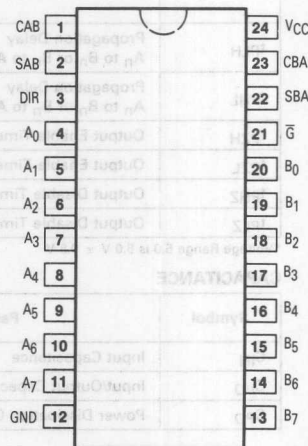
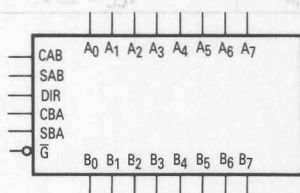


Figure 4

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA
- 'ACT646 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

- A₀-A₇** Data Register Inputs
A₀-A₇ Data Register A Outputs
B₀-B₇ Data Register B Inputs
B₀-B₇ Data Register B Outputs
CAB, CBA Clock Pulse Inputs
SAB, SBA Transmit/Receive Inputs
DIR, G Output Enable Inputs

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FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
\bar{G}	DIR	CAB	CBA	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	\downarrow	\downarrow	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

*The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

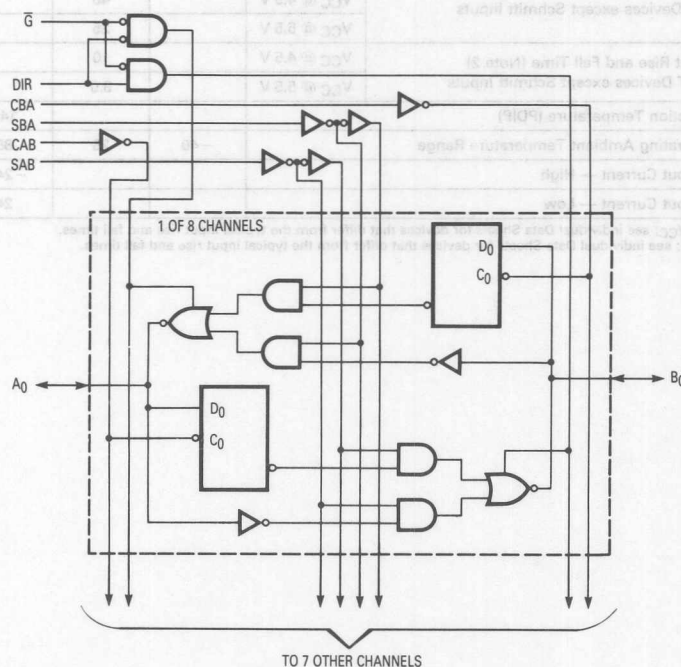
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

\downarrow = LOW-to-HIGH Transition

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC646 • MC74ACT646

MAXIMUM RATINGS*

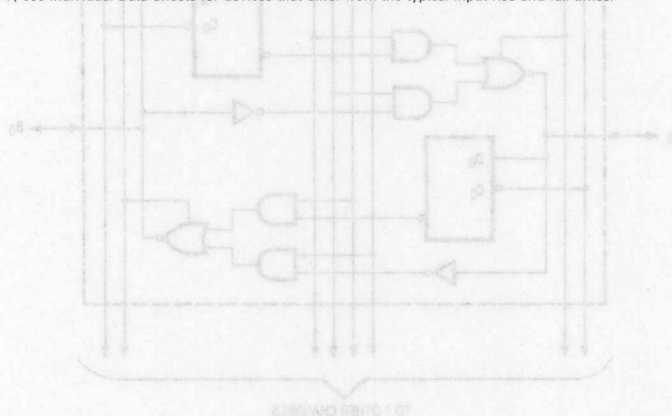
Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	ĀC	2.0	5.0	V
		ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) ĀC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	− 40	25	85	°C
I _{OH}	Output Current — High			− 24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

MC74AC646 • MC74ACT646

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC646 • MC74ACT646

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} [*] (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Clock to Bus	3.3 5.0	4.0 2.5	10.5 7.5	16.5 12	3.0 2.0	18.5 13	ns	3-6
t _{PHL}	Propagation Delay Clock to Bus	3.3 5.0	3.0 2.0	9.5 6.5	14.5 10.5	2.5 1.5	16 11.5	ns	3-6
t _{PLH}	Propagation Delay Bus to Bus	3.3 5.0	2.5 1.5	7.5 5.0	12 8.0	2.0 1.0	13.5 9.0	ns	3-5
t _{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	7.5 5.0	12.5 9.0	1.5 1.0	13.5 9.5	ns	3-5
t _{PLH}	Propagation Delay SBA or SAB to A _N or B _N (w/A _N or B _N HIGH or LOW)	3.3 5.0	2.0 1.5	8.5 6.0	13.5 10	1.5 1.5	15.5 11	ns	3-6
t _{PHL}	Propagation Delay SBA or SAB to A _N or B _N (w/A _N or B _N HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10	1.5 1.5	15 11	ns	3-6
t _{PZH}	Enable Time G̅ to A _N or B _N	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	2.0 1.5	12.5 9.0	ns	3-7
t _{PZL}	Enable Time G̅ to A _N or B _N	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	2.0 1.5	14 10	ns	3-8
t _{PHZ}	Disable Time G̅ to A _N or B _N	3.3 5.0	3.0 2.0	8.0 6.5	12.5 10	2.5 2.0	13.5 11	ns	3-7
t _{PLZ}	Disable Time G̅ to A _N or B _N	3.3 5.0	2.0 1.5	7.5 6.0	12 9.5	2.0 1.5	13.5 10.5	ns	3-8
t _{PZH}	Enable Time DIR to A _N or B _N	3.3 5.0	2.0 1.5	6.5 5.0	11 7.5	1.5 1.0	12 8.5	ns	3-7
t _{PZL}	Enable Time DIR to A _N or B _N	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.0	2.0 1.0	13 9.0	ns	3-8
t _{PHZ}	Disable Time DIR to A _N or B _N	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.5	1.5 1.5	12.5 10	ns	3-7
t _{PLZ}	Disable Time DIR to A _N or B _N	3.3 5.0	1.5 1.5	7.5 5.5	12 9.5	1.5 1.5	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup time, HIGH or LOW Bus to Clock	3.3	2.0	5.0	5.5	ns	3-9	
		5.0	1.5	4.0	4.5			
t _h	Hold Time, HIGH or LOW Bus to Clock	3.3	−1.5	0	0	ns	3-9	
		5.0	−0.5	0.5	1.0			
t _w	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5	4.5	ns	3-6	
		5.0	2.0	3.5	3.5			

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC646 • MC74ACT646

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5	3.0	16	ns	3-6
t _{PHL}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5	3.5	16	ns	3-6
t _{PLH}	Propagation Delay Bus to Bus	5.0	4.5	8.5	10.5	2.5	11.5	ns	3-5
t _{PHL}	Propagation Delay Bus to Bus	5.0	5.0	8.5	10.5	2.0	11.5	ns	3-5
t _{PLH}	Propagation Delay SBA or SAB to A _n or B _n (w/A _n or B _n HIGH or LOW)	5.0	5.0	9.5	11.5	2.5	12.5	ns	3-6
t _{PHL}	Propagation Delay SBA or SAB to A _n or B _n (w/A _n or B _n HIGH or LOW)	5.0	5.0	9.5	11.5	2.5	12.5	ns	3-6
t _{PZH}	Enable Time G̅ to A _n or B _n	5.0	6.0	9.0	11	1.5	12	ns	3-7
t _{PZL}	Enable Time G̅ to A _n or B _n	5.0	5.0	9.0	11	3.0	12	ns	3-8
t _{PHZ}	Disable Time G̅ to A _n or B _n	5.0	7.5	10.5	13	4.5	14.5	ns	3-7
t _{PLZ}	Disable Time G̅ to A _n or B _n	5.0	5.5	10.0	12.5	3.0	14.0	ns	3-8
t _{PZH}	Enable Time* DIR to A _n or B _n	5.0	5.5	6.5	10.5	1.5	11.5	ns	3-7
t _{PZL}	Enable Time DIR to A _n or B _n	5.0	4.0	6.5	10.5	3.0	11.5	ns	3-8
t _{PHZ}	Disable Time DIR to A _n or B _n	5.0	5.5	8.5	12.5	4.5	13.5	ns	3-7
t _{PLZ}	Disable Time DIR to A _n or B _n	5.0	4.0	8.5	12.5	3.0	13.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

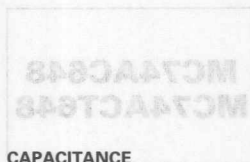
AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup time, HIGH or LOW Bus to Clock	5.0		7.0	8.0	ns	3-9	
t _h	Hold Time, HIGH or LOW Bus to Clock	5.0		2.5	2.5	ns	3-9	
t _w	Clock Pulse Width HIGH or LOW	5.0		4.5	8.0	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

MC74AC646 • MC74ACT646

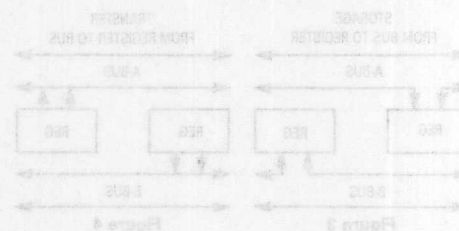
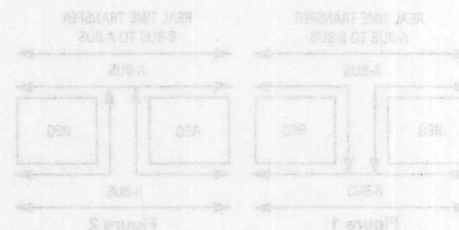


CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0 V
CPD	Power Dissipation Capacitance	60	pF	V _{CC} = 5.0 V

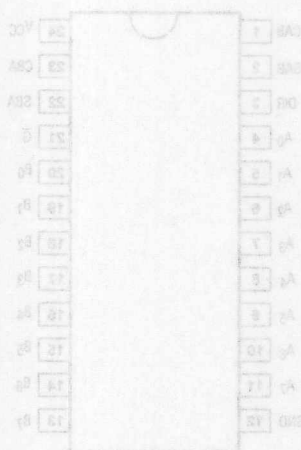


The MC74AC646 is a 3-state output buffer with two 8-bit registers. It is designed to interface with 8085 and 8086 microprocessors. The device features a 3-state output buffer that can be enabled or disabled by the output enable input (OE). The output buffer is capable of driving a load of up to 500 mA. The device is available in a 24-pin DIP package.



- Independent Registers for A and B Buses
- Multiplexed Real-Time and Storage Data Transfer
- Choice of Tri-State and Inverting Data Paths
- 3-State Outputs
- 500 mW Static Dissipation Package
- Outputs Sourcing/Sinking 54 mA

LOGIC SYMBOL



Pin Names

A0-A7: Data Register A Inputs

A8-A15: Data Register A Outputs

B0-B7: Data Register B Inputs

B8-B15: Data Register B Outputs

C: Clock Pulse Input

OE: Output Enable Input

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FACT DATA

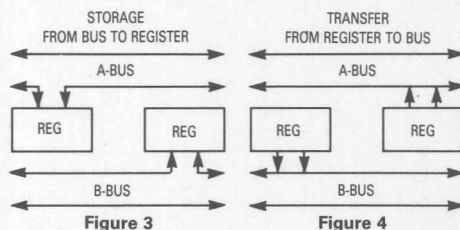
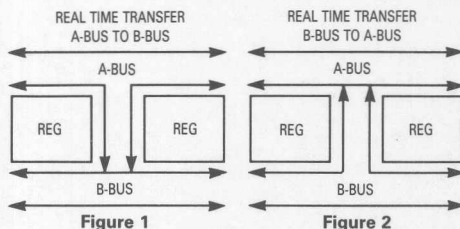


MC74AC648 MC74ACT648

Product Preview

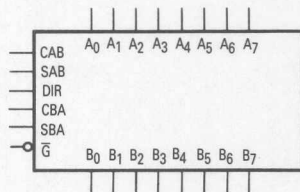
Octal Transceiver/Register with 3-State Outputs (Inverting)

The MC74AC648/74ACT648 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

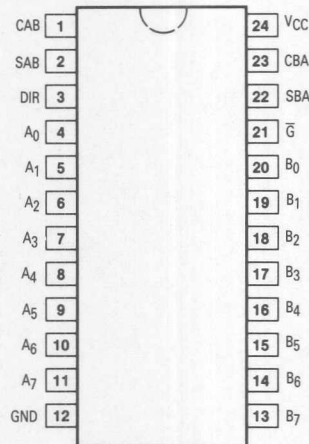
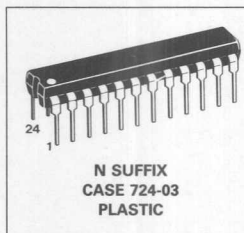


- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA

LOGIC SYMBOL



OCTAL
TRANSCIVER/REGISTER
WITH 3-STATE OUTPUTS
(INVERTING)



PIN NAMES

- A₀-A₇ Data Register Inputs
- DIR Data Register A Outputs
- B₀-B₇ Data Register B Inputs
- SAB Data Register B Outputs
- CAB, CBA Clock Pulse Inputs
- SAB, SBA Transmit/Receive Inputs
- DIR, \bar{G} Output Enable Inputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FACT DATA

MC74AC648 • MC74ACT648

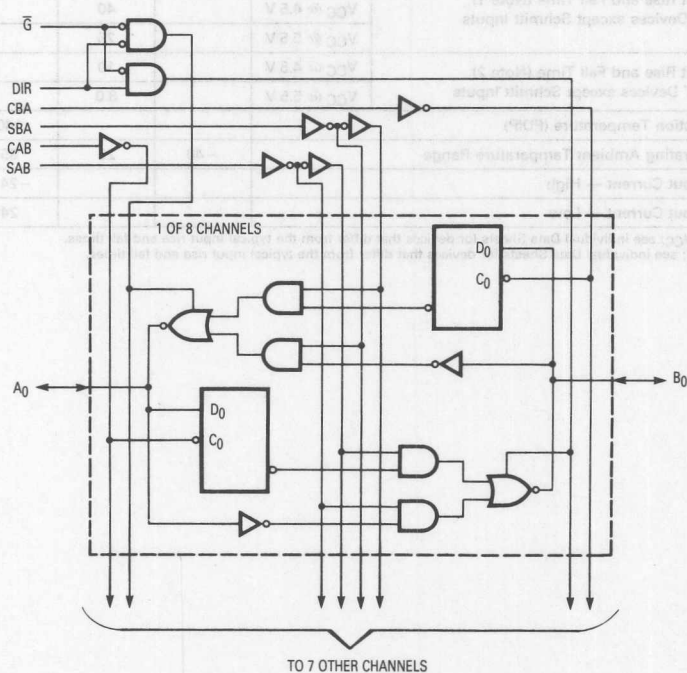
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
\overline{G}	DIR	CAB	CBA	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	
H	X	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time \overline{B} Data to A Bus Stored \overline{B} Data to A Bus
L	L	X	X	X	H	Output	Input	Real Time \overline{B} Data to A Bus Stored \overline{B} Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time \overline{A} Data to B Bus Stored \overline{A} Data to B Bus
L	H	H or L	X	H	X	Input	Output	Real Time \overline{A} Data to B Bus Stored \overline{A} Data to B Bus

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
┐ = LOW-to-HIGH Transition

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} \approx 3.0$ V	150		ns/V
		$V_{CC} \approx 4.5$ V	40		
		$V_{CC} \approx 5.5$ V	25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} \approx 4.5$ V	10		ns/V
		$V_{CC} \approx 5.5$ V	8.0		
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current — High			-24	mA
I_{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
 2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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ve limit ($\approx 5.5 \text{ V } V_{CC}$).

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions	
			T _A = +25°C		T _A = −40°C to +85°C				
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0				
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8				
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4				
					3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} −24 mA
					4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1				
					0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA
					0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} − 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80		μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.5 1.5	10 7.0	15.5 11	1.5 1.5	17 12	ns	3-6
t _{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10.5	1.5 1.5	14.5 11.5	ns	3-6
t _{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	6.0 4.0	10 7.0	1.5 1.0	11 7.5	ns	3-5
t _{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	5.5 3.5	9.0 7.5	1.5 1.0	10 8.0	ns	3-5
t _{PLH}	Propagation Delay SBA or SAB to A _N or B _N (w/A _N or B _N HIGH or LOW)	3.3 5.0	1.5 1.5	7.5 5.5	12.5 9.0	1.5 1.5	14 10	ns	3-6
t _{PHL}	Propagation Delay SBA or SAB to A _N or B _N (w/A _N or B _N HIGH or LOW)	3.3 5.0	1.5 1.5	7.5 5.5	12.5 9.5	1.5 1.5	14 10.5	ns	3-6
t _{PZH}	Enable Time G̅ to A _N or B _N	3.3 5.0	1.5 1.5	6.5 5.0	11 8.0	1.0 1.0	11.5 9.0	ns	3-7

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

AC CHARACTERISTICS — continued (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PZL}	Enable Time G̅ to A _N or B _N	3.3 5.0	1.5 1.5	7.0 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-8
t _{PHZ}	Disable Time G̅ to A _N or B _N	3.3 5.0	1.5 1.5	7.5 6.0	12 10	1.0 1.0	13 11	ns	3-7
t _{PLZ}	Disable Time G̅ to A _N or B _N	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.0 1.0	12.5 10	ns	3-8
t _{PZH}	Enable Time DIR to A _N or B _N	3.3 5.0	1.5 1.5	6.0 4.5	12.5 9.5	1.0 1.0	14 10.5	ns	3-7
t _{PZL}	Enable Time DIR to A _N or B _N	3.3 5.0	1.5 1.5	6.5 4.5	13 9.0	1.5 1.0	14.5 10.5	ns	3-8
t _{PHZ}	Disable Time DIR to A _N or B _N	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.0 1.0	13.5 10	ns	3-7
t _{PLZ}	Disable Time DIR to A _N or B _N	3.3 5.0	1.5 1.5	7.0 5.0	13.5 9.5	1.5 1.0	15 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	3.0 2.0	3.5 2.0	ns	3-9
t _h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	-1.5 -0.5	0 1.0	0 1.0	ns	3-9
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.0 3.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS — MC74ACT648
(Contact Local Motorola Sales Office)

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	65	pF	V _{CC} = 5.0 V

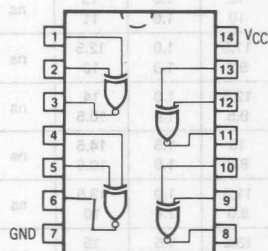


MOTOROLA

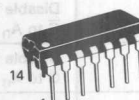
MC74AC810
MC74ACT810

Quad 2-Input Exclusive-NOR Gate

- Outputs Source/Sink 24 mA



QUAD 2-INPUT
EXCLUSIVE-NOR GATE



N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC810 • MC74ACT810

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) *AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) *ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	-40	25	85	°C
I _{OH}	Output Current — High			-24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} = -24 mA -24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

FACT DATA

MC74AC810 • MC74ACT810

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay Inputs to Outputs	3.3 5.0	1.0 1.0	8.5 7.5	12 9.0	1.0 1.0	13 9.5	ns	3-5
t _{PHL}	Propagation Delay Inputs to Outputs	3.3 5.0	1.0 1.0	9.5 6.5	12 9.0	1.0 1.0	13 10	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.0	8.5	10	1.0	10.5	ns	3-5
t _{PHL}	Propagation Delay	5.0	1.0	7.0	10	1.0	11	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
CPD	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V

FACT DATA



MC74AC825 MC74ACT825

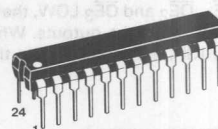
Product Preview 8-Bit D-Type Flip-Flop

The MC74AC825/74ACT825 is an 8-bit buffered register. It has Clock Enable and Clear features which are ideal for parity bus interfacing in high performance micro-programming systems. Also included are multiple enables that allow multi-use control of the interface.

The MC74AC825/74ACT825 is fully compatible with AMD's AM29825.

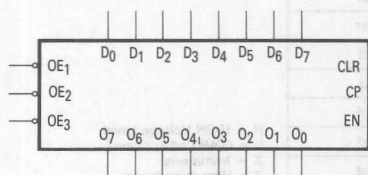
- Outputs Source/Sink 24 mA
- Inputs and Outputs are on Opposite Sides
- 'ACT825 Has TTL Compatible Inputs

8-BIT D-TYPE FLIP-FLOP



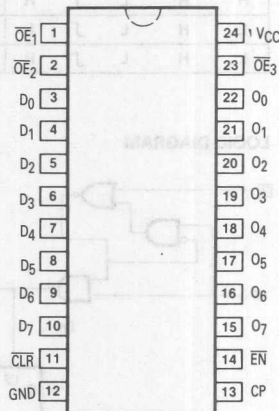
N SUFFIX
CASE 724-03
PLASTIC

LOGIC SYMBOL



PIN NAMES

- | | |
|---|----------------|
| D ₀ -D ₇ | Data Inputs |
| Q ₀ -Q ₇ | Data Outputs |
| OE ₁ , OE ₂ , OE ₃ | Output Enables |
| EN | Clock Enable |
| CLR | Clear |
| CP | Clock Input |



MC74AC825 • MC74ACT825

FUNCTIONAL DESCRIPTION

The MC74AC825/74ACT825 consists of eight D-type edge-triggered flip-flops. This device has 3-state outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE}_1 , \overline{OE}_2 and \overline{OE}_3 LOW, the contents of the flip-flops are available at the outputs. When one of \overline{OE}_1 , \overline{OE}_2 or \overline{OE}_3 is HIGH, the outputs go to the high impedance state.

Operation of the \overline{OE} input does not affect the state of the flip-flops. The MC74AC825/74ACT825 has Clear (CLR) and Clock Enable (EN) pins. These pins are ideal for parity bus interfacing in high performance systems.

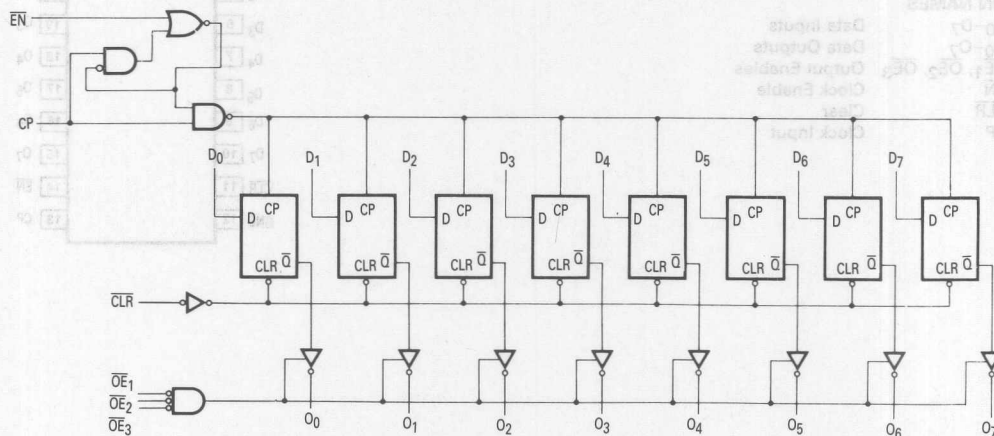
When CLR is LOW and \overline{OE} is LOW, the outputs are LOW. When CLR is HIGH, data can be entered into the flip-flops. When EN is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When EN is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
\overline{OE}	CLR	EN	CP	D _n	Q	O ('825)	\overline{O} ('826)	
H	X	L	J	L	L	Z	Z	High Z
H	X	L	J	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	J	L	L	Z	Z	Load
H	H	L	J	H	H	Z	Z	Load
L	H	L	J	L	L	L	H	Load
L	H	L	J	H	H	H	L	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
J = LOW-to-HIGH Transition
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

MC74AC825 • MC74ACT825

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC825 • MC74ACT825

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC825 • MC74ACT825

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC825 • MC74ACT825

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0						MHz	3-3
t _{PLH}	Propagation Delay CP to O _N	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CP to O _N	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CLR to O _N	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time OE to O _N	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time OE to O _N	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time OE to O _N	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time OE to O _N	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0					ns	3-9
t _s	Setup Time, HIGH or LOW EN to CP	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW EN to CP	3.3 5.0					ns	3-9
t _w	CP Pulse Width HIGH or LOW	3.3 5.0					ns	3-6
t _w	CLR Pulse Width, LOW	3.3 5.0					ns	3-6
t _{rec}	CLR to CP Recovery Time	3.3 5.0					ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC825 • MC74ACT825

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	120	158		109		MHz	3-3
t _{PLH}	Propagation Delay CP to O _n	5.0	1.5	5.5	9.5	1.5	10.5	ns	3-6
t _{PHL}	Propagation Delay CP to O _n	5.0	2.0	5.5	9.5	1.5	10.5	ns	3-6
t _{PHL}	Propagation Delay CLR to O _n	5.0	2.5	8.0	13.5	2.0	15.5	ns	3-6
t _{PZH}	Output Enable Time OE to O _n	5.0	1.5	6.0	10.5	1.5	11.5	ns	3-7
t _{PZL}	Output Enable Time OE to O _n	5.0	2.0	6.5	11.0	1.5	12.0	ns	3-8
t _{PHZ}	Output Disable Time OE to O _n	5.0	1.5	6.5	11.0	1.5	12.0	ns	3-7
t _{PLZ}	Output Disable Time OE to O _n	5.0	1.5	6.0	10.5	1.5	11.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	0.5	2.5	2.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	0	2.5	2.5	ns	3-9	
t _s	Setup Time, HIGH or LOW EN to CP	5.0	0	2.0	2.5	ns	3-9	
t _h	Hold Time, HIGH or LOW EN to CP	5.0	0	1.0	1.0	ns	3-9	
t _w	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	5.5	ns	3-6	
t _w	CLR Pulse Width, LOW	5.0	3.0	5.5	5.5	ns	3-6	
t _{rec}	CLR to CP Recovery Time	5.0	1.5	3.5	4.0	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	44	pF	V _{CC} = 5.0 V



MOTOROLA

MC74AC843 MC74ACT843

Product Preview

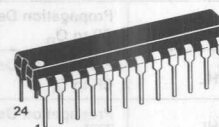
9-Bit Transparent Latch

The MC74AC843/74ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The MC74AC843/74ACT843 is functionally and pin compatible with AMD's AM29843.

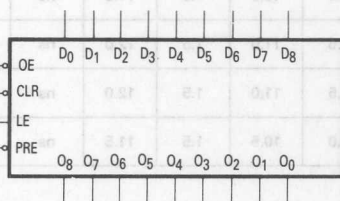
- 'ACT843 Has TTL Compatible Inputs

9-BIT
TRANSPARENT
LATCH



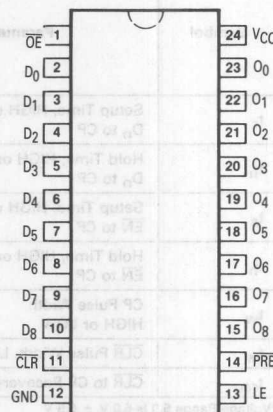
N SUFFIX
CASE 724-03
PLASTIC

LOGIC SYMBOL



PIN NAMES

D₀-D₈ Data Inputs
O₀-O₈ Data Outputs
OE Output Enable
LE Latch Enable
CLR Clear
PRE Preset



Symbol	Parameter	Value Typ	Units	Test Condition
C _{in}	Input Capacitance	4.5	pf	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	5.0	pf	V _{CC} = 5.0 V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FACT DATA

5-338

MC74AC843 • MC74ACT843

FUNCTIONAL DESCRIPTION

The MC74AC843/74ACT843 consists of nine D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high

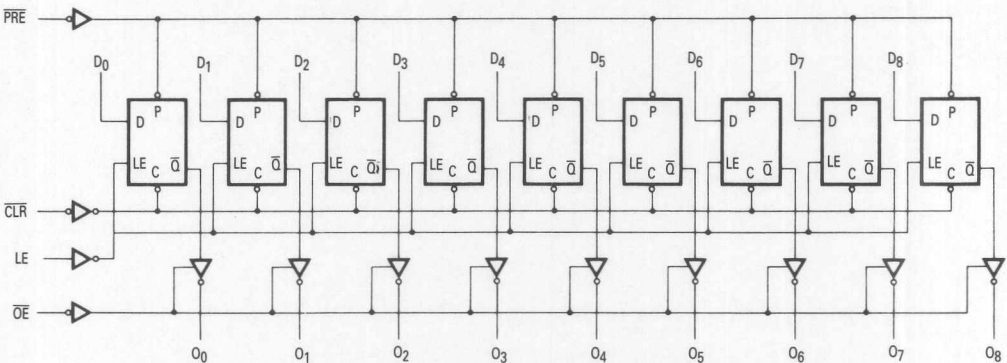
impedance state. In addition to the LE and \overline{OE} pins, the MC74AC843/74ACT843 has a Clear (CLR) pin and a Preset (PRE) pin. These pins are ideal for parity bus interfacing in high performance systems. When CLR is LOW, the outputs are LOW if \overline{OE} is LOW. When CLR is HIGH, data can be entered into the latch. When PRE is LOW, the outputs are HIGH if \overline{OE} is LOW. Preset overrides CLR.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
CLR	PRE	\overline{OE}	LE	D	Q	O ('843)	\overline{O} ('844)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

MC74AC843 • MC74ACT843

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

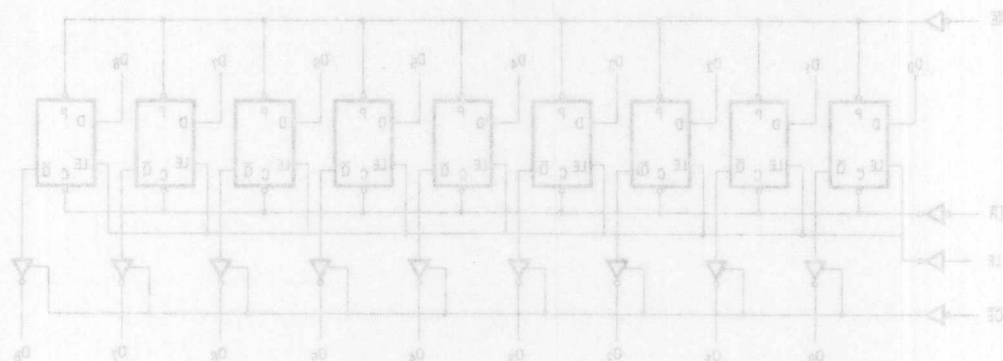
*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

5



This diagram is provided for the understanding of logic operation and should not be used to estimate propagation delays.

FACT DATA

MC74AC843 • MC74ACT843

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0						ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0						ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay PRE to O _n	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CLR to O _n	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time OE to O _n	3.3 5.0						ns	3-8
t _{PHL}	Propagation Delay PRE to O _n	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay CLR to O _n	3.3 5.0						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0					ns	3-9
t _w	LE Pulse Width, HIGH	3.3 5.0					ns	3-6
t _w	PRE Pulse Width, LOW	3.3 5.0					ns	3-6
t _w	CLR Pulse Width, LOW	3.3 5.0					ns	3-6
t _{rec}	PRE Recovery Time	3.3 5.0					ns	3-9
t _{rec}	CLR Recovery Time	3.3 5.0					ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	5.0						ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	5.0						ns	3-5
t _{PLH}	Propagation Delay LE to O _n	5.0						ns	3-6
t _{PHL}	Propagation Delay LE to O _n	5.0						ns	3-6
t _{PLH}	Propagation Delay PRE to O _n	5.0						ns	3-6
t _{PHL}	Propagation Delay CLR to O _n	5.0						ns	3-6
t _{PZH}	Output Enable Time OE to O _n	5.0						ns	3-7
t _{PZL}	Output Enable Time OE to O _n	5.0						ns	3-8
t _{PHZ}	Output Disable Time OE to O _n	5.0						ns	3-7
t _{PLZ}	Output Disable Time OE to O _n	5.0						ns	3-8
t _{PHL}	Propagation Delay PRE to O _n	5.0						ns	3-6
t _{PLH}	Propagation Delay CLR to O _n	5.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	5.0				ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to LE	5.0				ns	3-9	
t _w	LE Pulse Width, HIGH	5.0				ns	3-6	
t _w	PRE Pulse Width, LOW	5.0				ns	3-6	
t _w	CLR Pulse Width, LOW	5.0				ns	3-6	
t _{rec}	PRE Recovery Time	5.0				ns	3-9	
t _{rec}	CLR Recovery Time	5.0				ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance		pF	V _{CC} = 5.0 V

FACT DATA



MOTOROLA

Product Preview

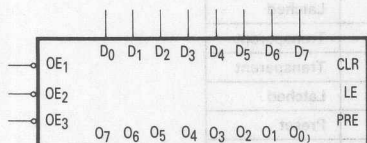
8-Bit Transparent Latch

The MC74AC845/74ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple OE controls.

The MC74AC845/74ACT845 is functionally and pin compatible with AMD's AM29845.

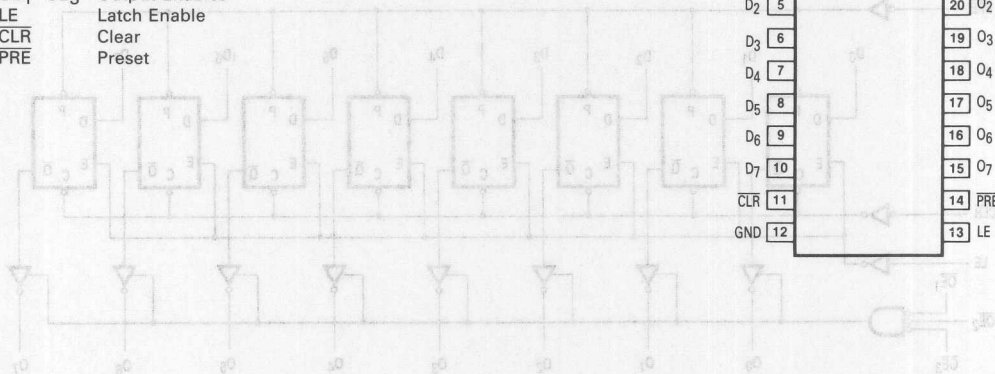
- 'ACT845 Has TTL Compatible Inputs

LOGIC SYMBOL



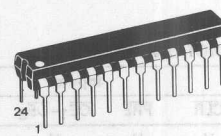
PIN NAMES

- D₀-D₇ Data Inputs
- O₀-O₇ Data Outputs
- OE₁-OE₃ Output Enables
- LE Latch Enable
- CLR Clear
- PRE Preset



**MC74AC845
MC74ACT845**

**8-BIT
TRANSPARENT
LATCH**



**N SUFFIX
CASE 724-03
PLASTIC**

FUNCTIONAL DESCRIPTION

The MC74AC845/74ACT845 consists of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW

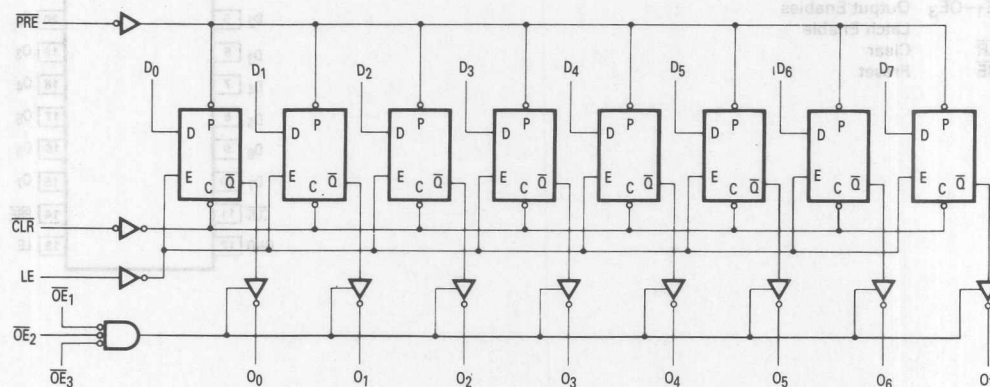
transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enables (\overline{OE}_1 , \overline{OE}_2 , \overline{OE}_3) are LOW. When any one of \overline{OE}_1 , \overline{OE}_2 or \overline{OE}_3 is HIGH, the bus output is in the high impedance state.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
CLR	PRE	\overline{OE}_1 – \overline{OE}_3	LE	D	Q	O ('845)	\overline{O} ('846)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FACT DATA

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	150		ns/V
		V _{CC} @ 4.5 V	40		
		V _{CC} @ 5.5 V	25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	10		ns/V
		V _{CC} @ 5.5 V	8.0		
T _J	Junction Temperature (PDIP)			140	°C
T _A	Operating Ambient Temperature Range	−40	25	85	°C
I _{OH}	Output Current — High			−24	mA
I _{OL}	Output Current — Low			24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} – 12 mA	
		4.5		3.86	3.76		I _{OH} – 24 mA	
		5.5		4.86	4.76		– 24 mA	
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA	
		4.5		0.36	0.44		I _{OL} 24 mA	
		5.5		0.36	0.44		24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8		V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4		V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76		V	*V _{IN} = V _{IL} or V _{IH} −24 mA −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1		V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} − 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

Symbol	Parameter	V _{CC} (V)	74ACT		Units
			T _A = +25°C C _L = 50 pF	T _A = -40°C C _L = 50 pF	
t _{SD}	Setup Time, HIGH or LOW	5.5	2.0	2.0	ns
t _H	Hold Time, HIGH or LOW	5.5	2.0	2.0	ns
t _W	1.5 Pulse Width, HIGH	5.5	2.0	2.0	ns
t _W	PRE Pulse Width, LOW	5.5	2.0	2.0	ns
t _W	CLR Pulse Width, LOW	5.5	2.0	2.0	ns
t _{REC}	PRE Recovery Time	5.5	2.0	2.0	ns
t _{REC}	CLR Recovery Time	5.5	2.0	2.0	ns

*Voltage range 5.0 to 5.5 V ± 0.3 V
Voltage range 5.0 to 5.5 V ± 0.3 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC* (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _N to O _N	3.3 5.0						ns	3-5
t _{PHL}	Propagation Delay D _N to O _N	3.3 5.0						ns	3-5
t _{PLH}	Propagation Delay LE to O _N	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay LE to O _N	3.3 5.0						ns	3-6
t _{PLH}	Propagation Delay PRE to O _N	3.3 5.0						ns	3-6
t _{PHL}	Propagation Delay CLR to O _N	3.3 5.0						ns	3-6
t _{PZH}	Output Enable Time OE to O _N	3.3 5.0						ns	3-7
t _{PZL}	Output Enable Time OE to O _N	3.3 5.0						ns	3-8
t _{PHZ}	Output Disable Time OE to O _N	3.3 5.0						ns	3-7
t _{PLZ}	Output Disable Time OE to O _N	3.3 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0					ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0					ns	3-9
t _w	LE Pulse Width, HIGH	3.3 5.0					ns	3-6
t _w	$\overline{\text{PRE}}$ Pulse Width, LOW	3.3 5.0					ns	3-6
t _w	$\overline{\text{CLR}}$ Pulse Width, LOW	3.3 5.0					ns	3-6
t _{rec}	$\overline{\text{PRE}}$ Recovery Time	3.3 5.0					ns	3-9
t _{rec}	$\overline{\text{CLR}}$ Recovery Time	3.3 5.0					ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

FACT DATA

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	5.0						ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	5.0						ns	3-5
t _{PLH}	Propagation Delay LE to O _n	5.0						ns	3-6
t _{PHL}	Propagation Delay LE to O _n	5.0						ns	3-6
t _{PLH}	Propagation Delay PRE to O _n	5.0						ns	3-6
t _{PHL}	Propagation Delay CLR to O _n	5.0						ns	3-6
t _{PZH}	Output Enable Time OE to O _n	5.0						ns	3-7
t _{PZL}	Output Enable Time OE to O _n	5.0						ns	3-8
t _{PHZ}	Output Disable Time OE to O _n	5.0						ns	3-7
t _{PLZ}	Output Disable Time OE to O _n	5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	5.0					ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	5.0					ns	3-9
t _w	LE Pulse Width, HIGH	5.0					ns	3-6
t _w	PRE Pulse Width, LOW	5.0					ns	3-6
t _w	CLR Pulse Width, LOW	5.0					ns	3-6
t _{rec}	PRE Recovery Time	5.0					ns	3-9
t _{rec}	CLR Recovery Time	5.0					ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	44	pF	V _{CC} = 5.0 V



MOTOROLA

MC74AC4020

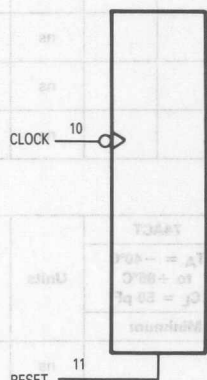
14-Stage Binary Ripple Counter

The MC74AC4020 consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4020 for some designs.

- 140 MHz Typ. Clock
- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity

LOGIC DIAGRAM



PIN 16 = VCC
PIN 8 = GND

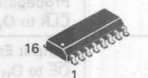
FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

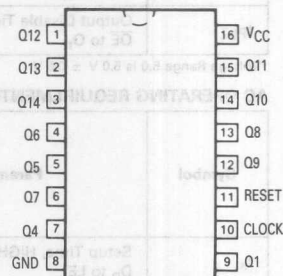
14-STAGE BINARY RIPPLE COUNTER



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**



MC74AC4020

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
P_D	Power Dissipation in Still Air Plastic** SOIC Package**	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

**Derating: Plastic DIP: -10 mW/°C from 65°C to 125°C
SOIC Package: -7.0 mW/°C from 65°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}/V_{out}	Input Voltage, Output Voltage (Ref. to GND)	0	V_{CC}	
T_A	Operating Temperature, All Package Types	-40	+85	°C
t_r/t_f	Input Rise/Fall Time (Figure 1)	0	150 40 25	ns/V

$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA
$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA	$V_{in} = V_{CC}$ 1.5 mA	$V_{out} = V_{CC}$ 1.5 mA

MC74AC4020

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Unit	
I_{CC}	Maximum Quiescent Supply Voltage	80	μA	$V_{in} = V_{CC}$ or GND $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{in} = V_{CC}$ or GND $V_{CC} = 5.5 V$, $T_A = 25^\circ C$

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5		2.1 3.15 3.85	2.1 3.15 3.85	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5		0.9 1.35 1.65	0.9 1.35 1.65	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
V _{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I _{OUT} = −50 μA	
		3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
V _{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I _{OUT} = 50 μA	
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	Minimum Dynamic Output Current**	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	

*All outputs loaded; thresholds on input associated with output under test.

**Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC4020



AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	110 130	0 140		100 120		MHz	
t _{PLH}	Propagation Delay CP to Q1	3.3 5.0	2.0 2.0		11 8.0	2.0 2.0	14 10	ns	
t _{PHL}	Propagation Delay CP to Q1	3.3 5.0	2.0 2.0		11 8.0	2.0 2.0	14 10	ns	
t _{PLH}	Propagation Delay CP to Q4	3.3 5.0	2.0 2.0		18 13	2.0 2.0	21 16	ns	
t _{PHL}	Propagation Delay CP to Q4	3.3 5.0	2.0 2.0		18 13	2.0 2.0	21 16	ns	
t _{PHL}	Propagation Delay Reset to any Q	3.3 5.0	3.0 3.0		12 10	3.0 3.0	15 12	ns	
t _{PHL}	Propagation Delay Q _n to Q _n + 1	3.3 5.0	0 0		5.5 3.5	0 0	6.5 4.5	ns	
t _{PHL}	Propagation Delay Q _n to Q _n + 1	3.3 5.0	0 0		5.5 3.5	0 0	6.5 4.5	ns	
t _{rec} MR to CP	Recovery Time	3.3 5.0	0 0	−2.5 −1.5		0 0		ns	
t _w CP	Minimum Pulse Width Clock Pin	3.3 5.0	4.0 3.0	3.5 2.5		4.5 3.5		ns	
t _w MR	Minimum Pulse Width Master Reset	3.3 5.0	4.0 3.0	3.5 2.5		4.5 3.5		ns	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V



MOTOROLA

MC74AC4040

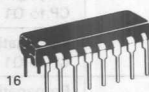
12-Stage Binary Ripple Counter

The MC74AC4040 consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4040 for some designs.

- 140 MHz Typ. Clock
- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity

**12-STAGE
BINARY RIPPLE
COUNTER**

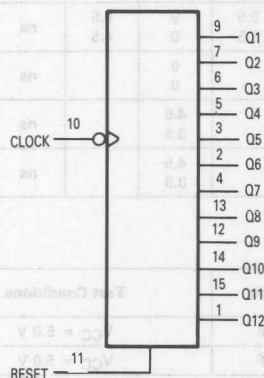


**N SUFFIX
CASE 648-08
PLASTIC**

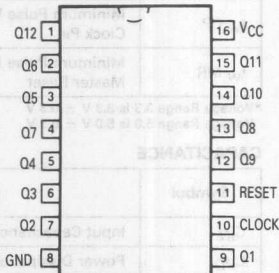


**D SUFFIX
CASE 751B-03
PLASTIC**

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND



FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

FACT DATA

5-356

MC74AC4040

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
P_D	Power Dissipation in Still Air Plastic** SOIC Package**	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

**Derating: Plastic DIP: -10 mW/°C from 65°C to 125°C

SOIC Package: -7.0 mW/°C from 65°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}/V_{out}	Input Voltage, Output Voltage (Ref. to GND)	0	V_{CC}	
T_A	Operating Temperature, All Package Types	-40	+85	°C
t_r/t_f	Input Rise/Fall Time (Figure 1)	0	150	ns/V
	$V_{CC} = 3.0$ V	0	40	
	$V_{CC} = 4.5$ V	0	25	
	$V_{CC} = 5.5$ V	0	25	

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Unit	
I_{CC}	Maximum Quiescent Supply Voltage	80	μA	$V_{in} = V_{CC}$ or GND $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{in} = V_{CC}$ or GND $V_{CC} = 5.5 V$, $T_A = 25^\circ C$

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0		2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5		3.15	3.15			
		5.5		3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0		0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5		1.35	1.35			
		5.5		1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} - 24 mA - 24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		± 0.5	± 5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	
I _{OLD}	Minimum Dynamic Output Current**	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			- 75	mA	V _{OHD} = 3.85 V Min	

*All outputs loaded; thresholds on input associated with output under test.

**Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC4040

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	110 130	120 140		100 120		MHz	
n _{CP} to Q1	Propagation Delay n _{CP} to Q1	3.3 5.0	2.0 2.0		11 8.0	2.0 2.0	14 10	ns	
Q _n to Q _n + 1	Propagation Delay Q _n to Q _n + 1	3.3 5.0	0 0		5.5 3.5	0 0	6.5 4.5	ns	
MR to Q t _{HL}	Propagation Delay MR to Q	3.3 5.0	3.0 3.0		12 10	3.0 3.0	15 12	ns	
t _{rec} n _{CP} to MR	Recovery Time	3.3 5.0	0 0	− 2.5 − 1.5		0 0		ns	
t _w n _{CP}	Minimum Pulse Width Clock Pin	3.3 5.0	4.0 3.0	3.5 2.5		4.5 3.5		ns	
t _w MR	Minimum Pulse Width Master Reset	3.3 3.0	4.0 3.0	3.5 2.5		4.5 3.5		ns	

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V

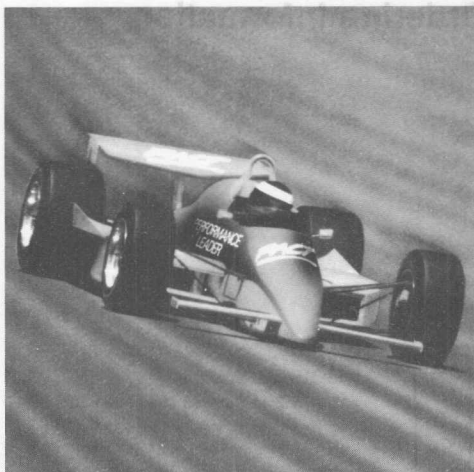
AC CHARACTERISTICS (See Figures and Waveforms — See Section 3)

Symbol	Parameter	VCC ^a (V)	TAC			TMC			Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C C _L = 50 pF				
			Min	Typ	Max	Min	Max			
t _{max}	Maximum Clock Frequency	3.3 2.0	170 120	120 140		100 120		MHz		
t _{pc} to Q1	Propagation Delay ncp to Q1	3.3 2.0	2.0 2.0		1.1 0.8		2.0 1.0		ns	
t _{pc} to Qn+1	Propagation Delay Qn to Qn+1	3.3 2.0	0 0		0.8 0.3		0 0		ns	
t _{MR} to Q	Propagation Delay MR to Q	3.3 2.0	2.0 2.0		1.1 1.0		2.0 1.0		ns	
t _{rec} to MR	Recovery Time ncp to MR	3.3 2.0	0 0	-1.8			0 0		ns	
t _W nCP	Minimum Pulse Width Clock Pin	3.3 2.0	4.0 3.0	3.0 2.0			4.0 3.0		ns	
t _W MR	Minimum Pulse Width Master Reset	3.3 2.0	1.0 1.0	3.0 2.0			4.0 3.0		ns	

^a Voltage Range 2.2 to 2.3 V ± 0.3 V
Voltage Range 2.0 to 2.1 V ± 0.2 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{in}	Input Capacitance	4.0	pF	VCC = 2.0 V
C _{pd}	Power Dissipation Capacitance	20	pF	VCC = 2.0 V



Package Outlines and Ordering Information

Ordering Information

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used in form part of a simplified purchasing code where the package type and temperature range are defined as follows:

MCATAC

Temperature Range Family
 MCATAC = Commercial FACT
 MCATAC = Commercial TTL-Compatible Advanced
 CMOS

Device Type

Package Code
 N = Plastic DIP
 D = Narrow SOIC
 DW = Wide SOIC

Package Outlines

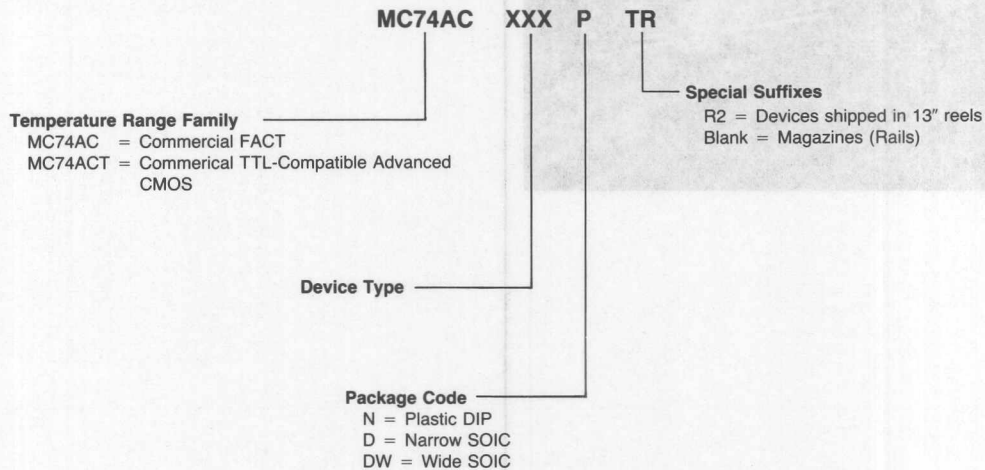
The package codes indicated above are shown in the detailed outline drawings in this section.

Package Outlines and Ordering Information

Package Outlines and Ordering Information

Ordering Information

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



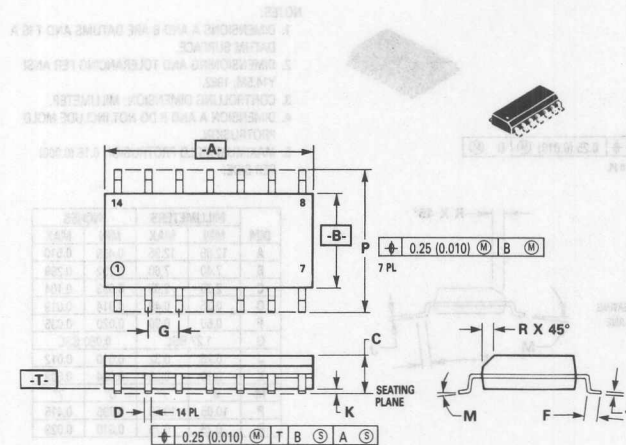
Package Outlines

The package codes indicated above are shown in the detailed outline drawings in this section.

PACKAGE OUTLINES

(bump) SOIC

Case 751A-02 D Suffix 14-Pin Plastic SO-14

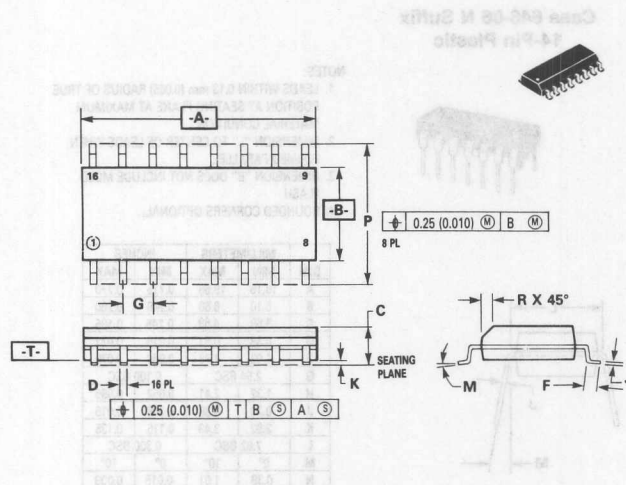


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Case 751B-03 D Suffix 16-Pin Plastic SO-16



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

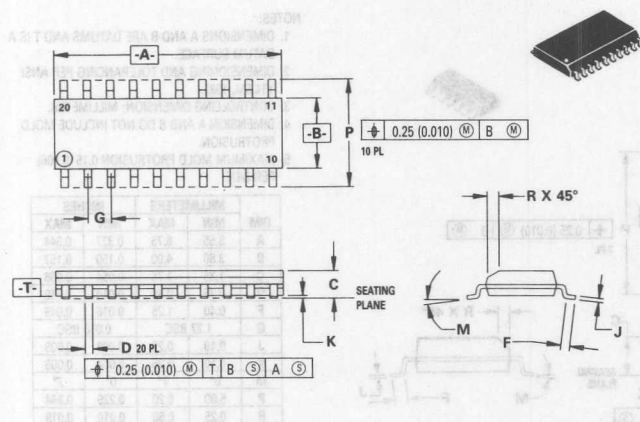
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

FACT DATA

PACKAGE OUTLINES

SOIC (continued)

Case 751D-03 DW Suffix 20-Pin Plastic SO-20



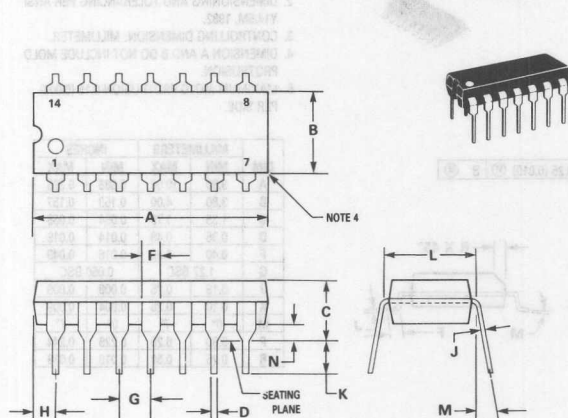
NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PLASTIC DUAL-IN-LINE

Case 646-06 N Suffix 14-Pin Plastic



NOTES:

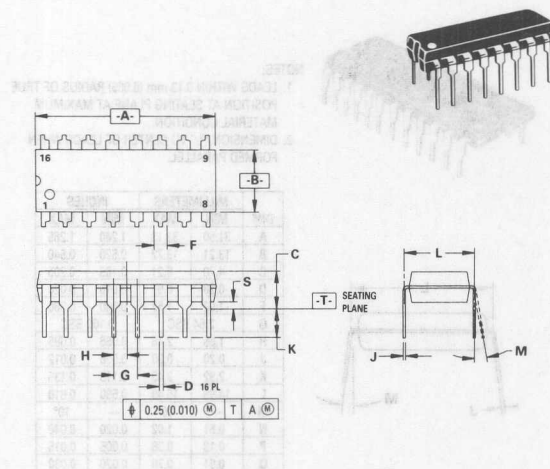
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

FACT DATA

PLASTIC DUAL-IN-LINE (continued)

Case 648-08 N Suffix 16-Pin Plastic

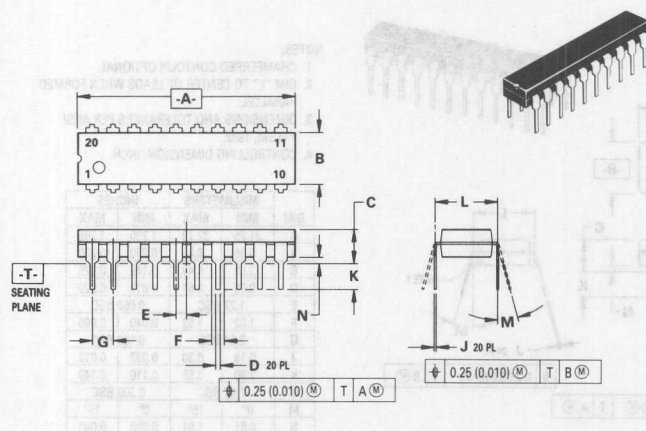


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 738-03 N Suffix 20-Pin Plastic



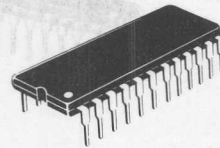
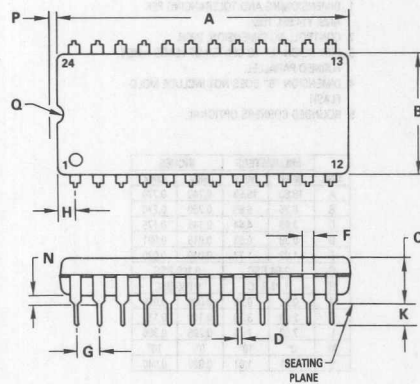
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

PLASTIC DUAL-IN-LINE (continued)

Case 649-03 N Suffix 24-Pin Plastic

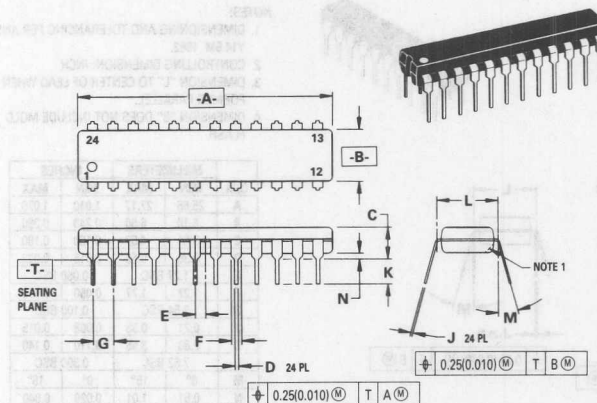


NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

Case 724-03 24-Pin Plastic



NOTES:

- CHAMFERED CONTOUR OPTIONAL.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040